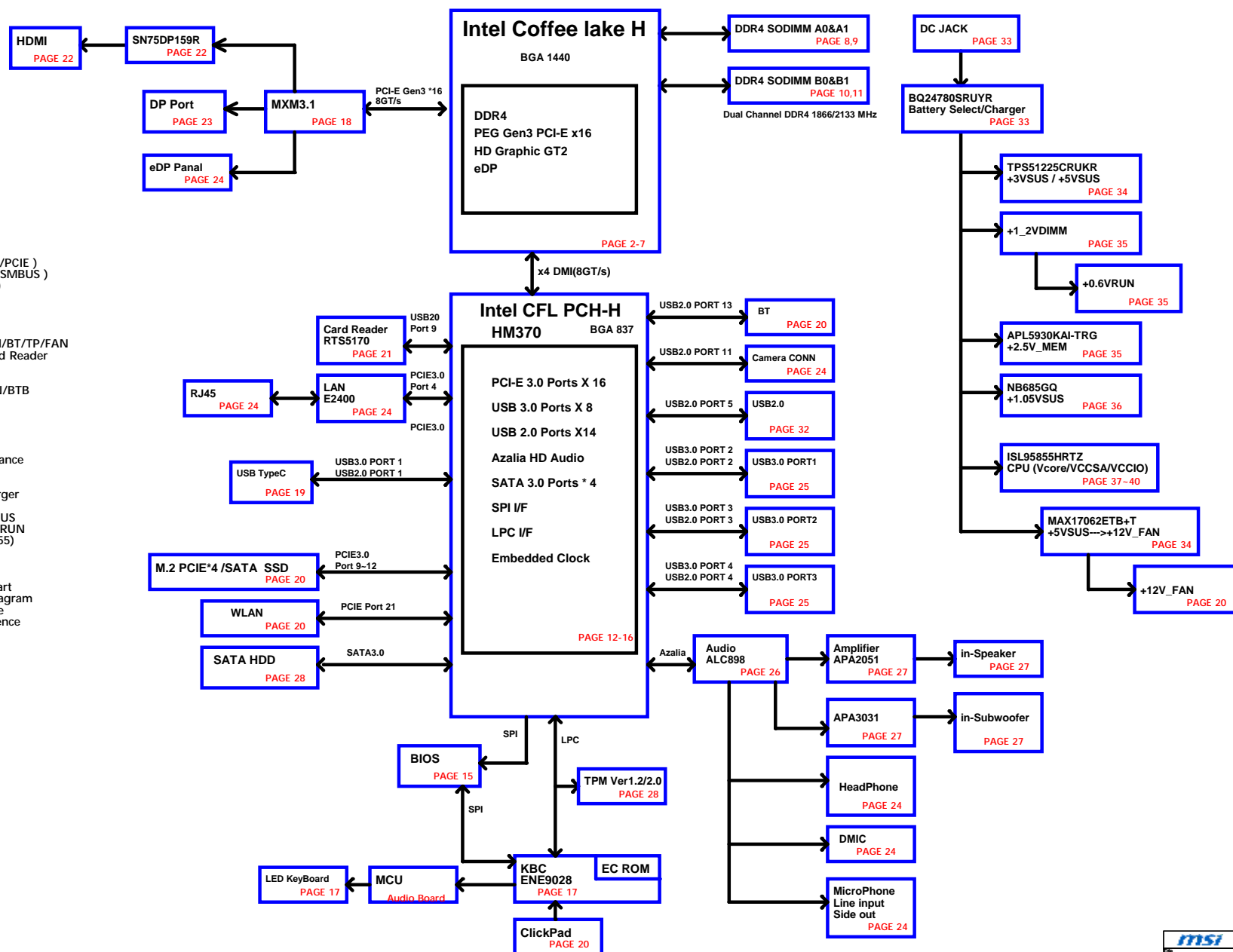
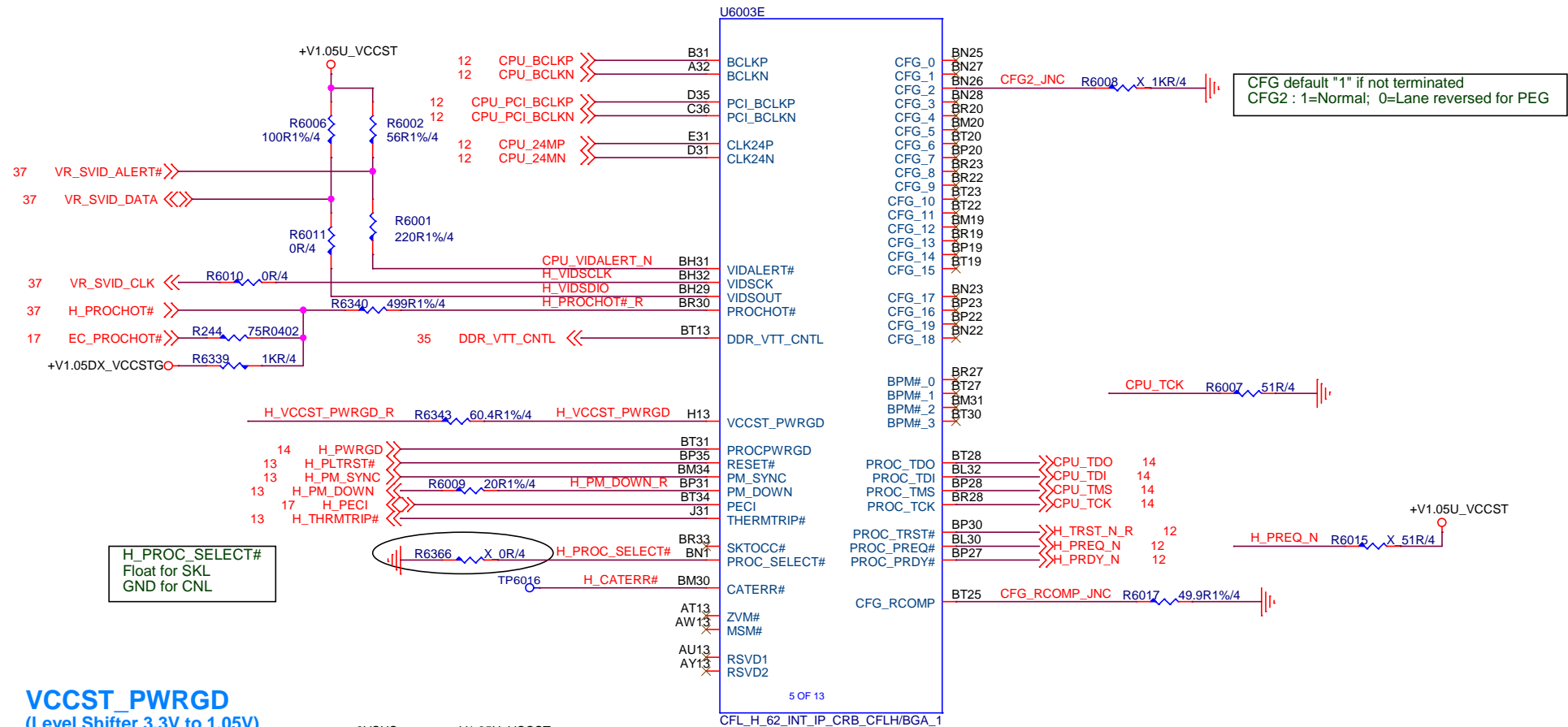


MS-16L41 Ver:0A Intel Coffee Lake Platform

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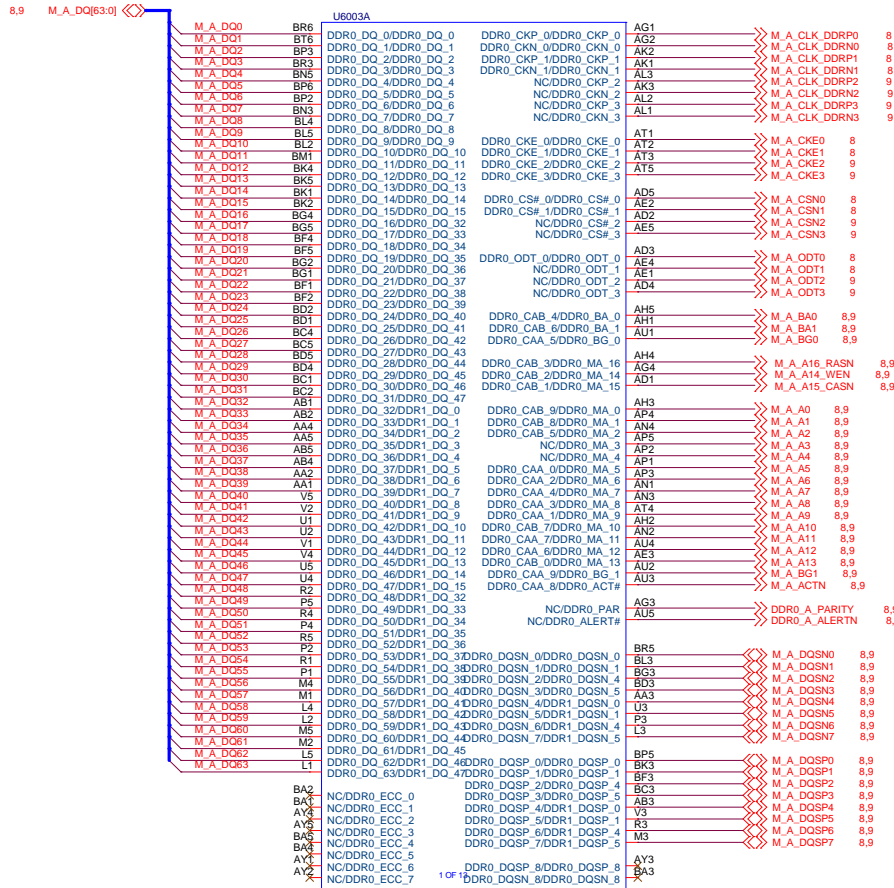


CFL-H (HOST)

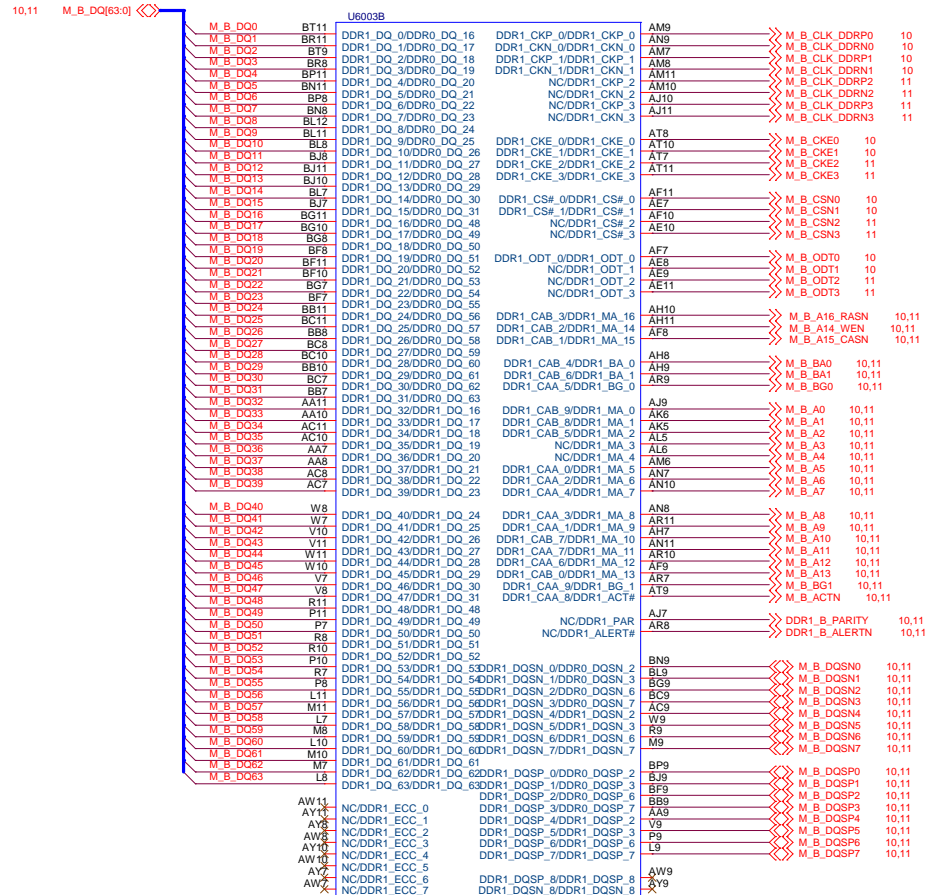


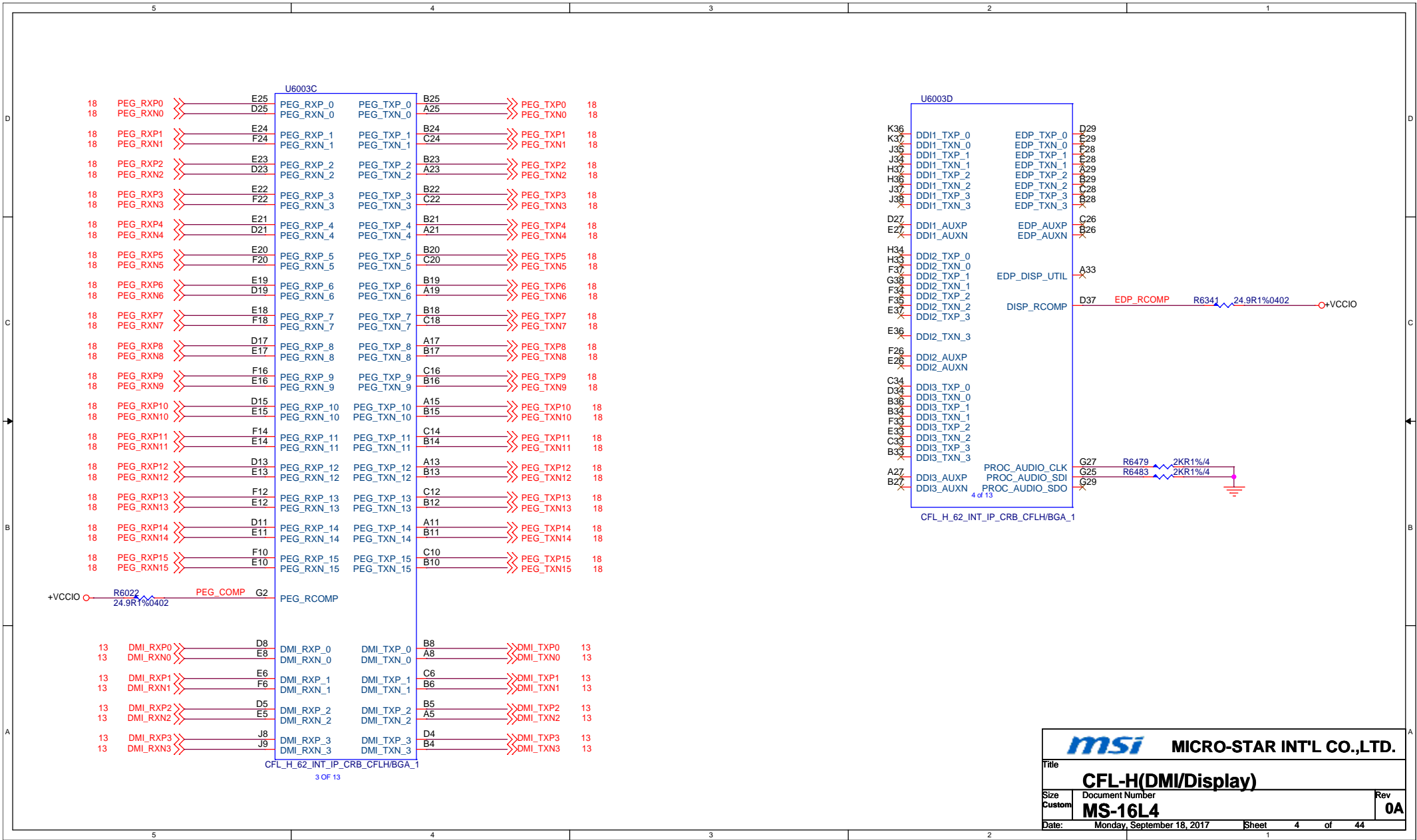
msi MICRO-STAR INT'L CO.,LTD.	
Title CFL-H(HOST)	
Size Custom	Document Number MS-16L4
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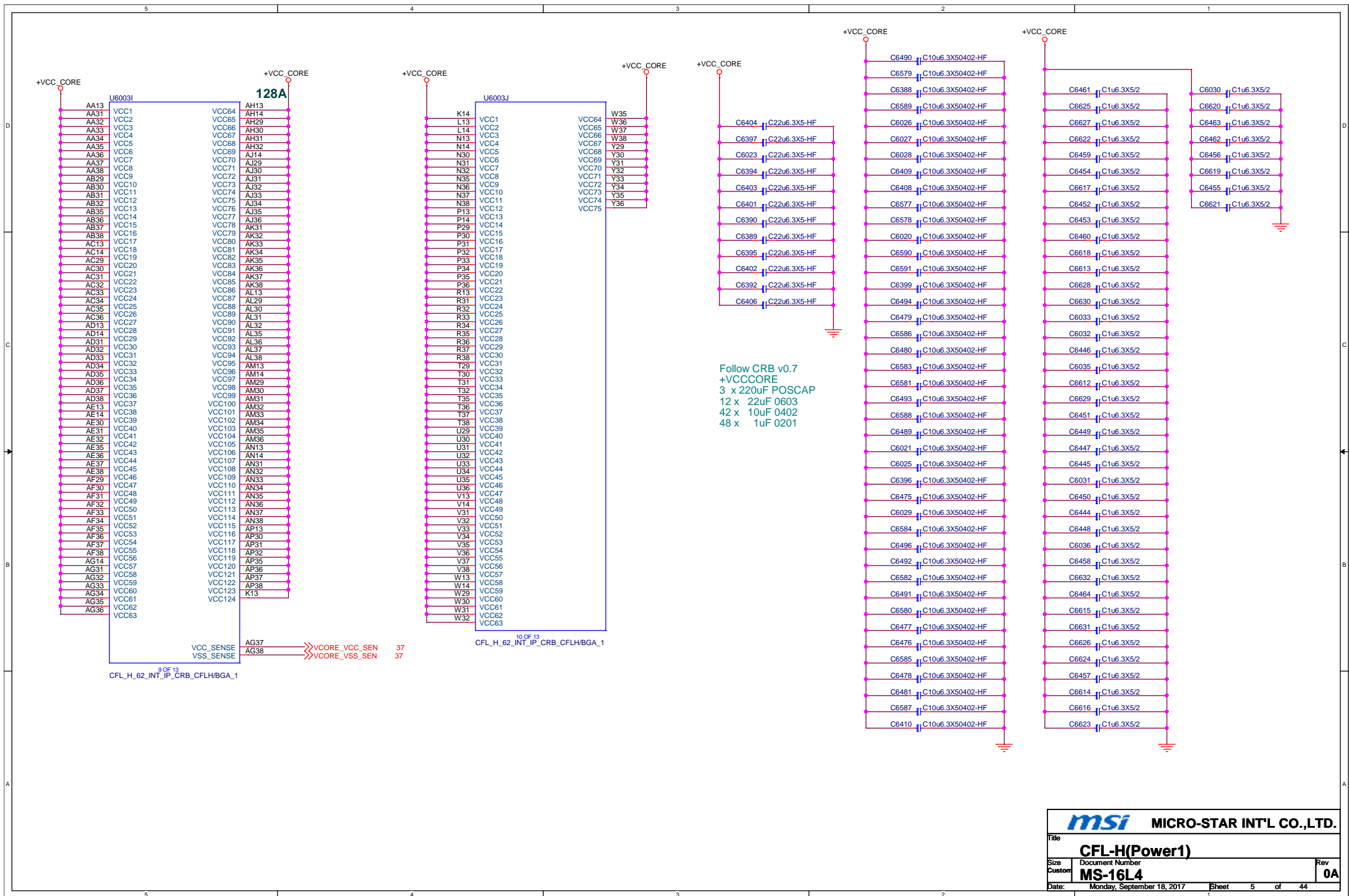
DDR Channel A



DDR Channel B

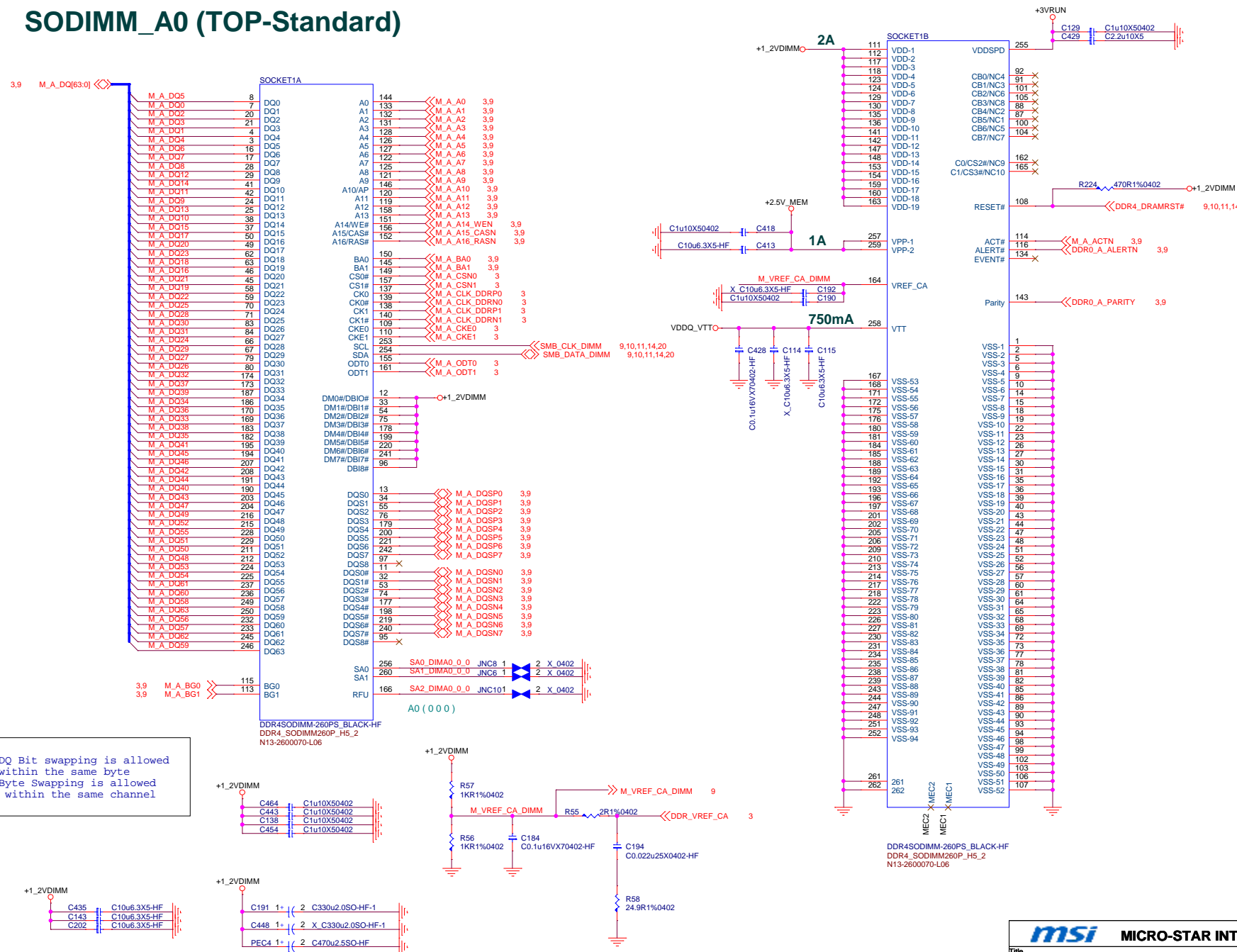






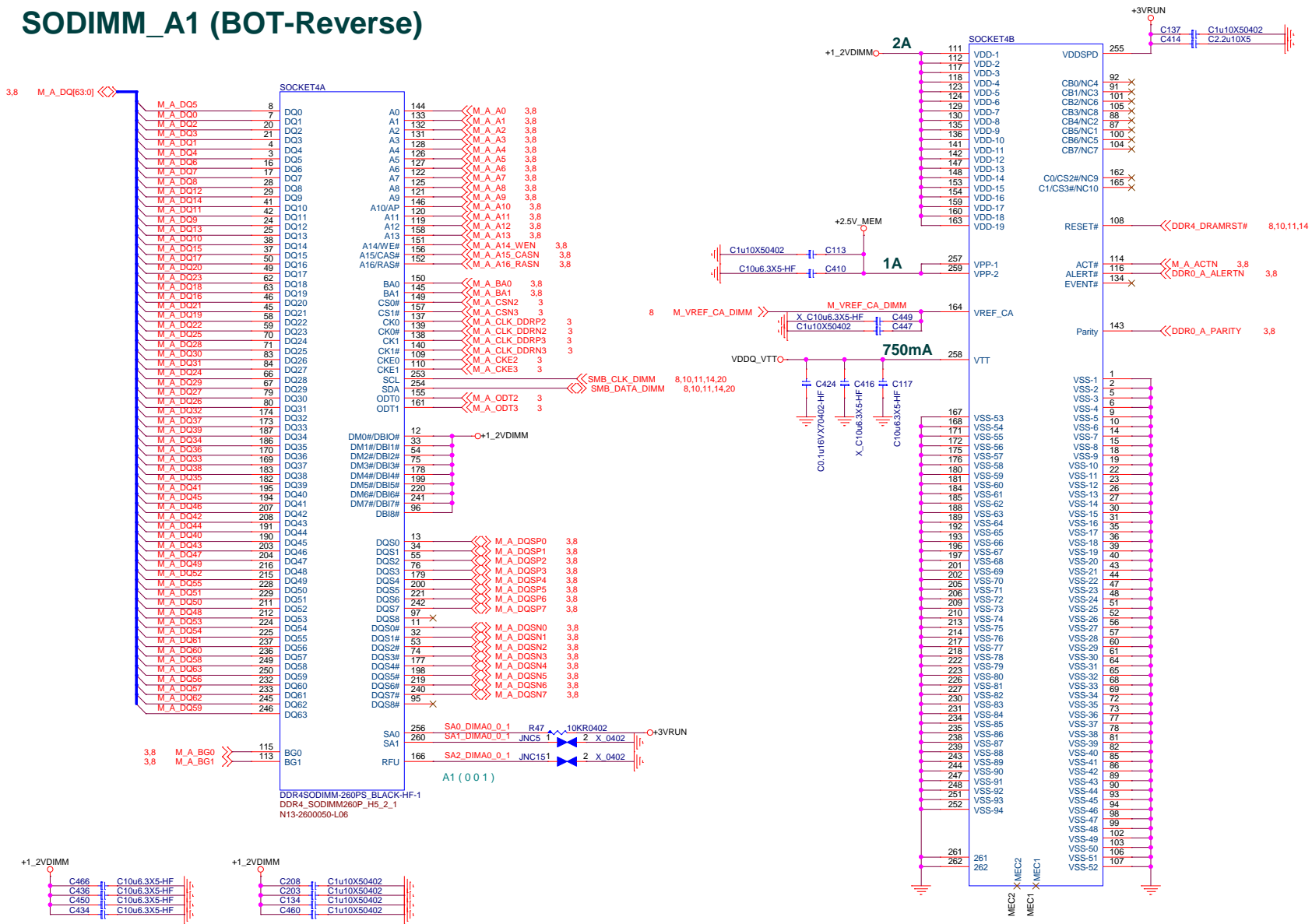
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A10	VSS_1	VSS_82	AK4							AW5	VSS_163	VSS_244	BJ15							BN4	VSS_325	VSS_409	F15						AT14	VCCGT1	VCCGT80	BD35																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																		

SODIMM_A0 (TOP-Standard)

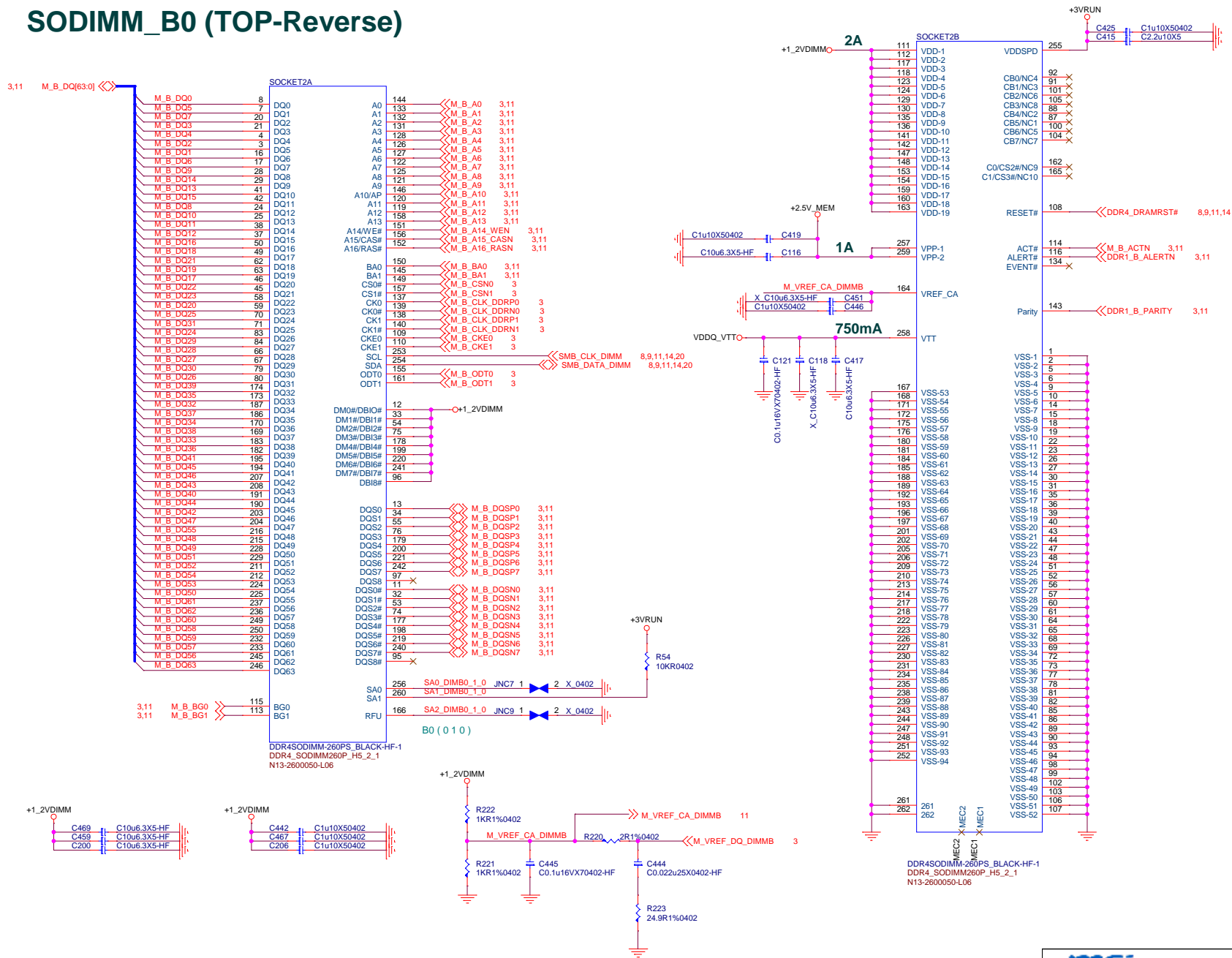


DQ Bit swapping is allowed within the same byte
Byte Swapping is allowed within the same channel

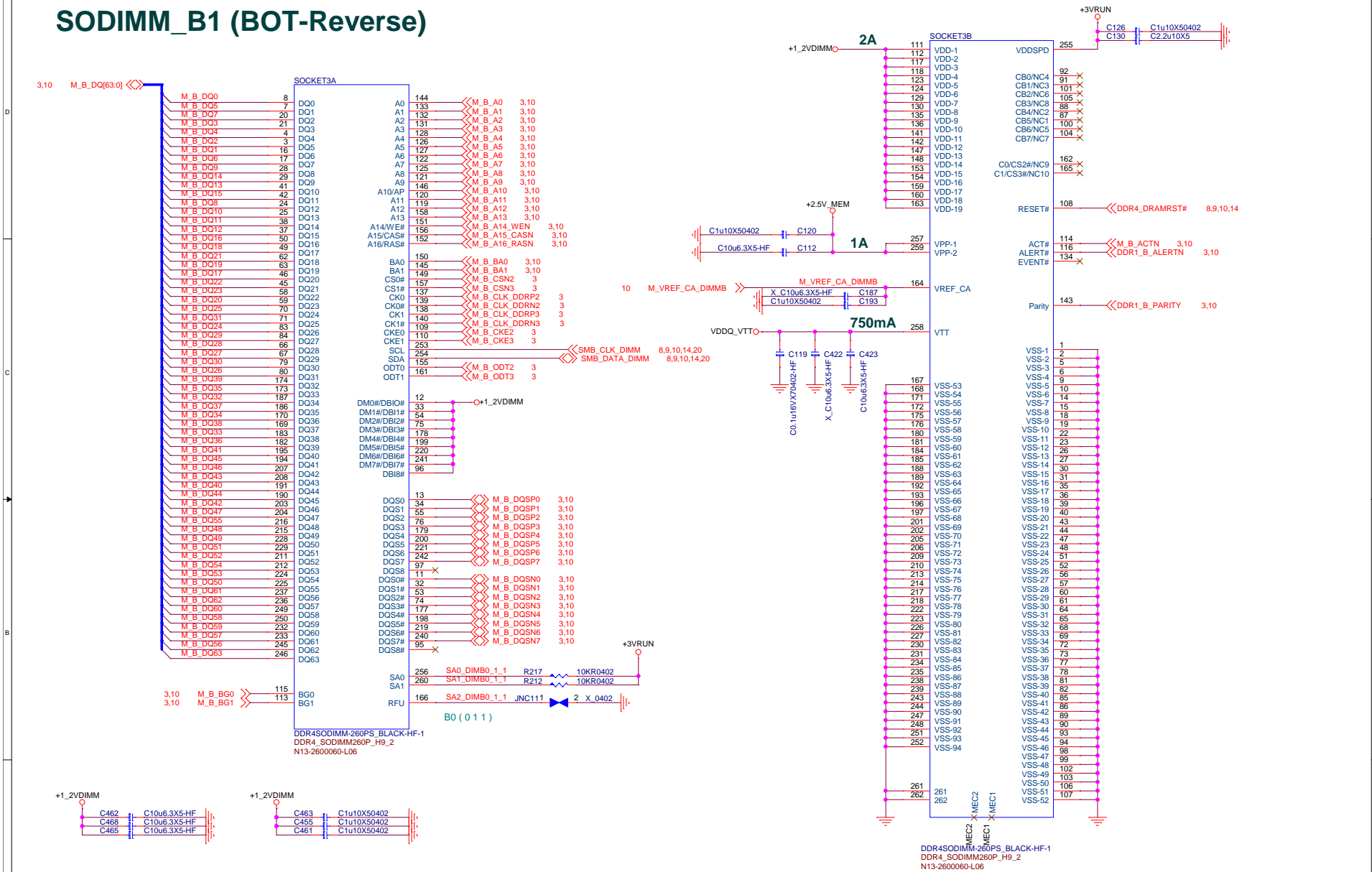
SODIMM_A1 (BOT-Reverse)



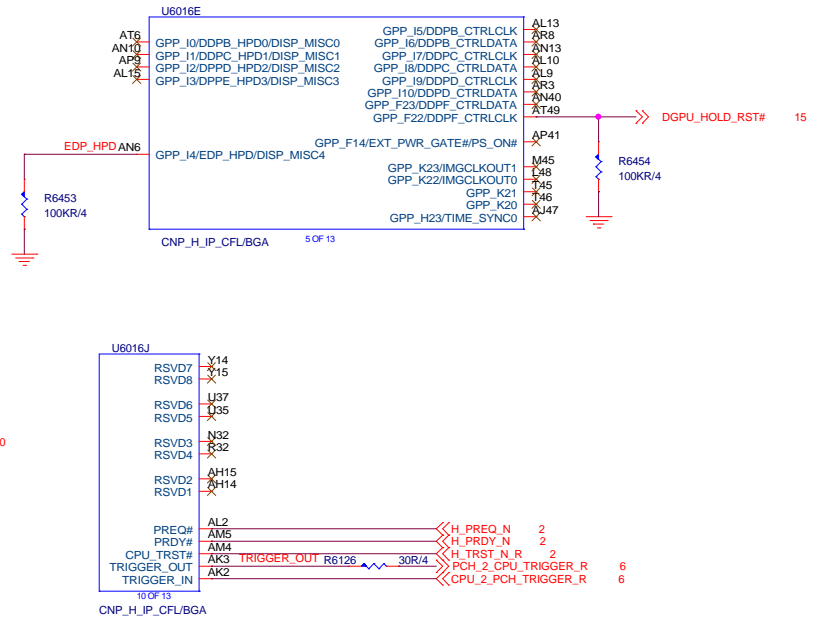
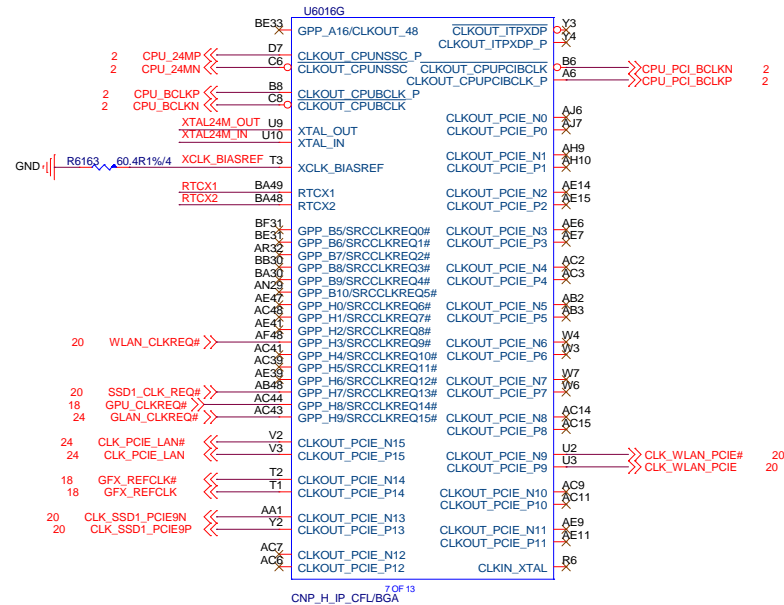
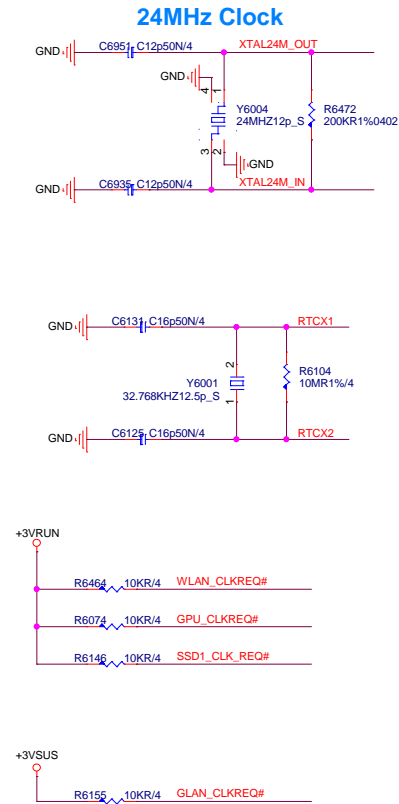
SODIMM_B0 (TOP-Reverse)



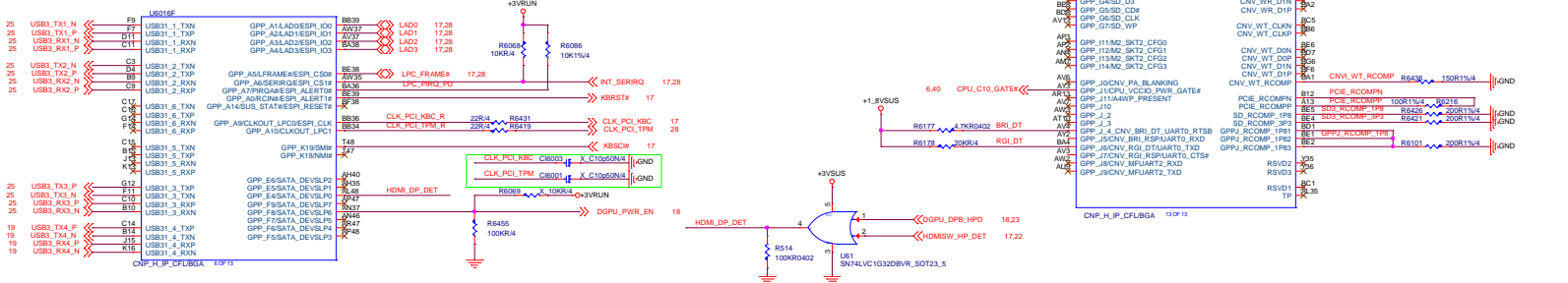
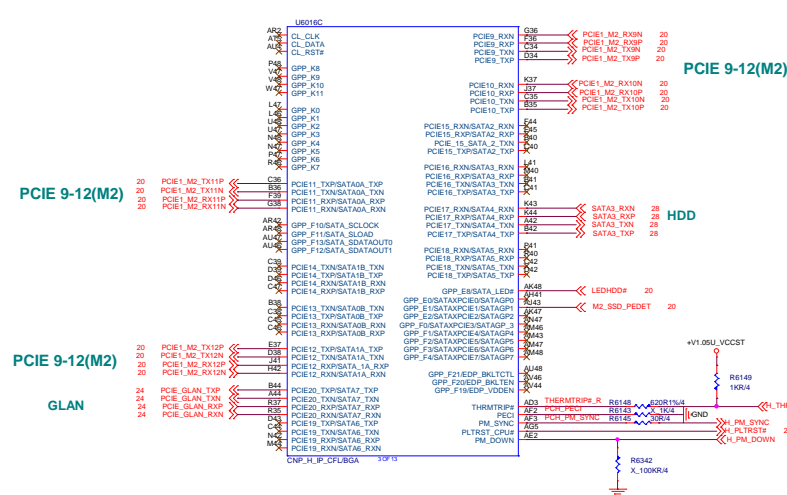
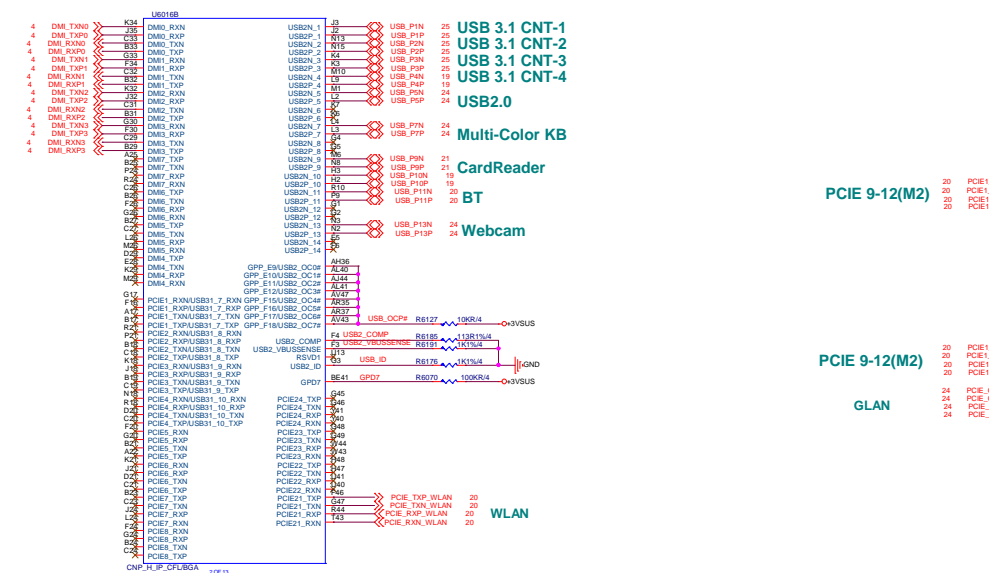
SODIMM_B1 (BOT-Reverse)



HM370 (RTC/Clock)



HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)



GPD

External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

GPP J4

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

GPP J6

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP J9

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

HM370 (HDA/GPIO/JAG)

Functional Strap Definitions

HDA_SDO

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)

SMBALERT# / GPP_C2

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

SML0ALERT# / GPP_C5

This signal has a weak internal pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

SML1ALERT# / PCHHOT# / GPP_B23

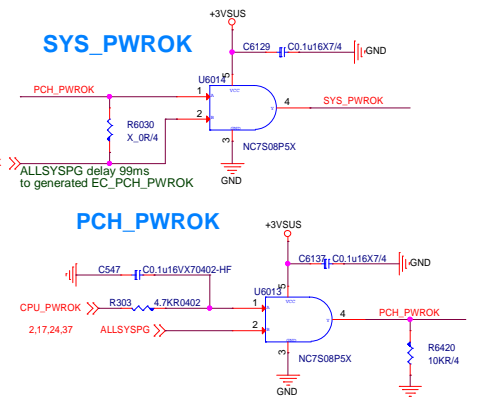
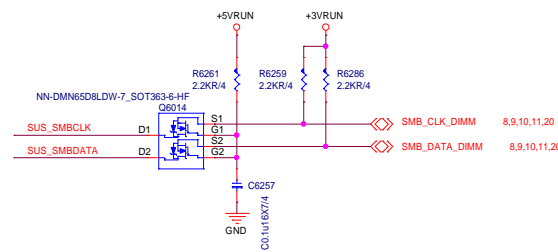
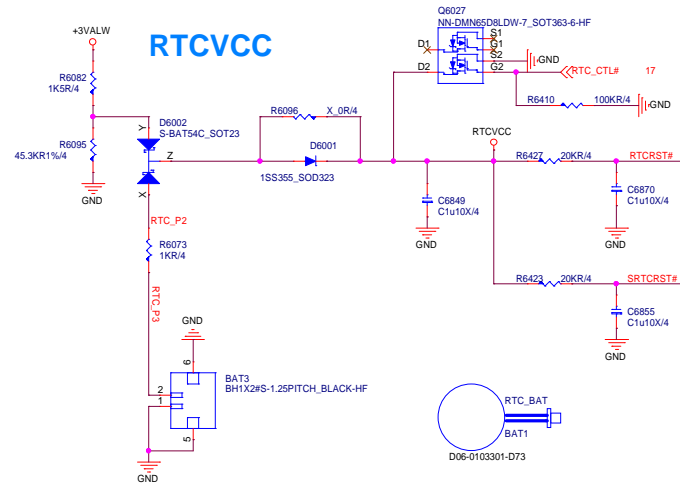
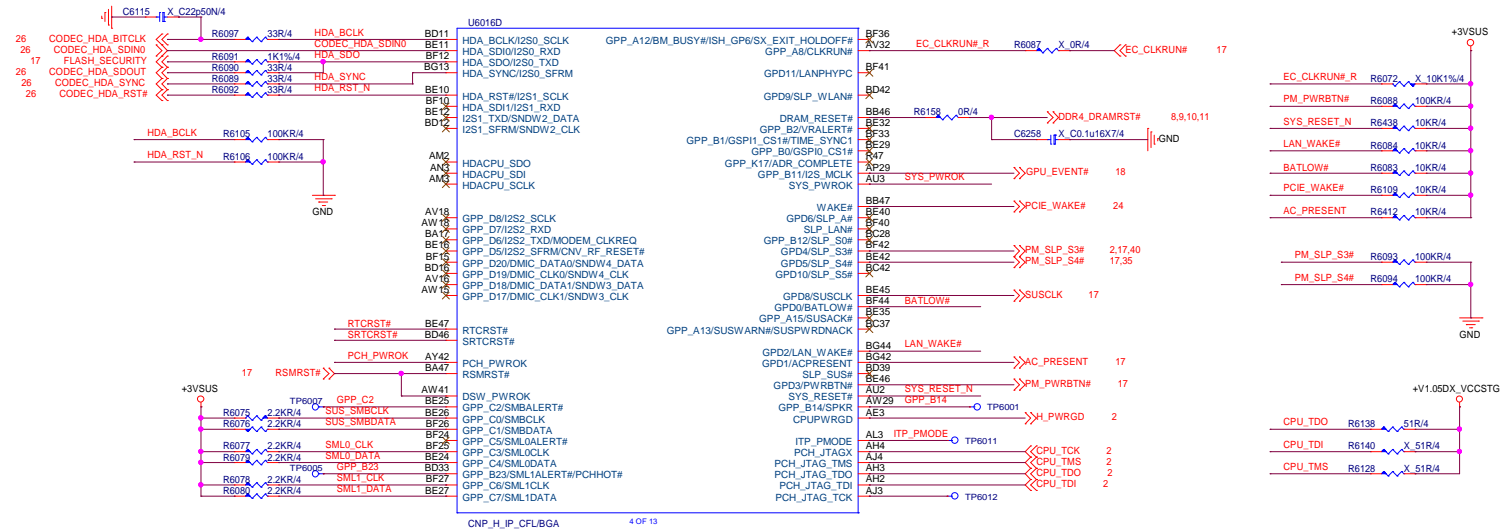
This signal has an internal pull-down.

DG/ RTC Well Input Strap

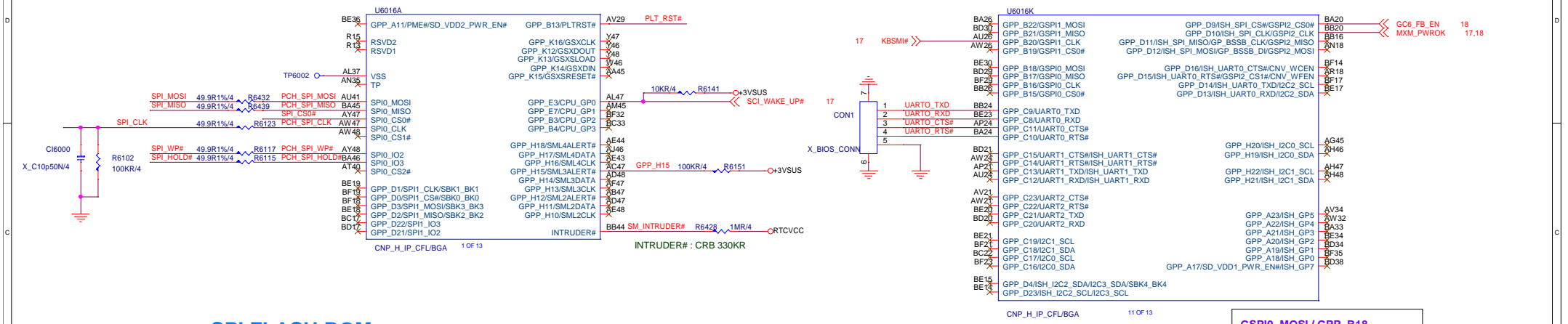
RSMRST# & DSW_PWROK, PCH_PWROK : PD
RTCRST#, SRTCST#, INTRUDER# : PU

SPKR / GPP_B14

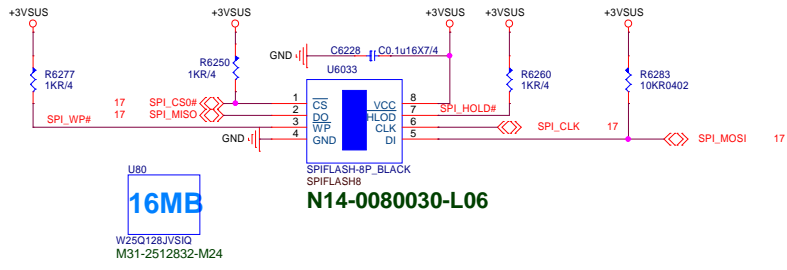
The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)



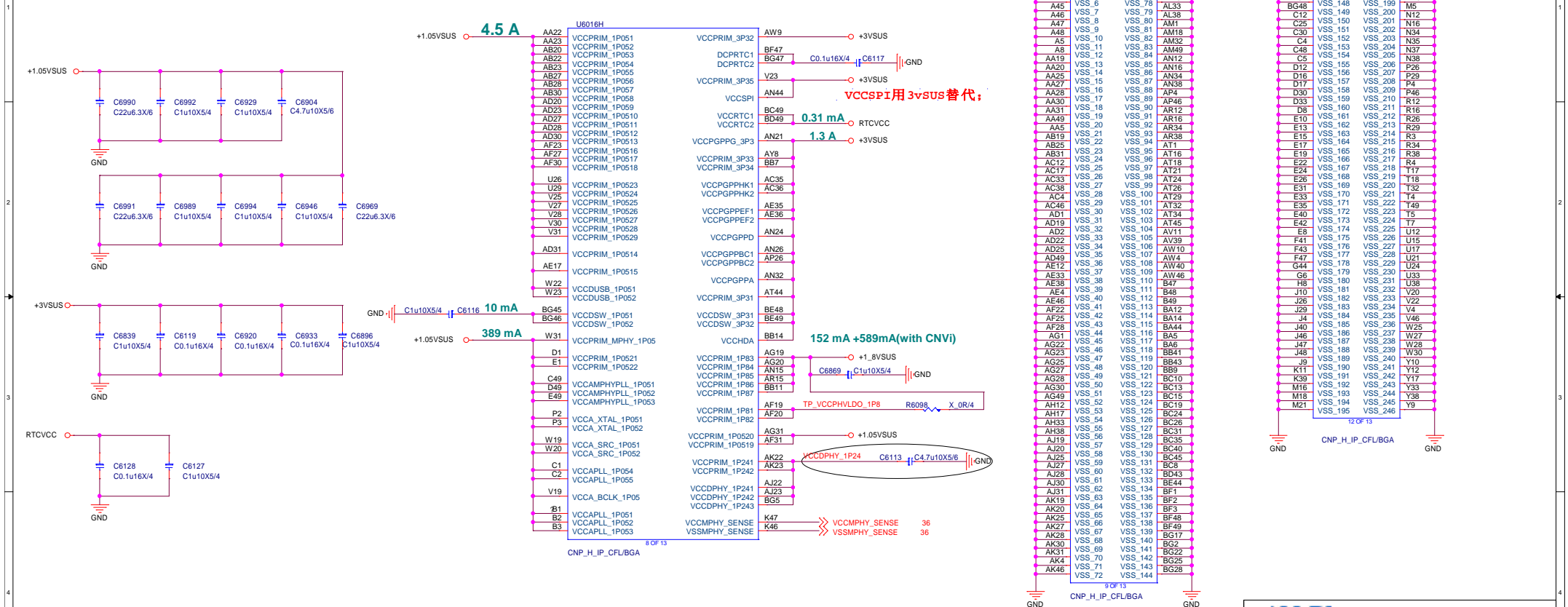
HM370 (UART/I2C/SPI)



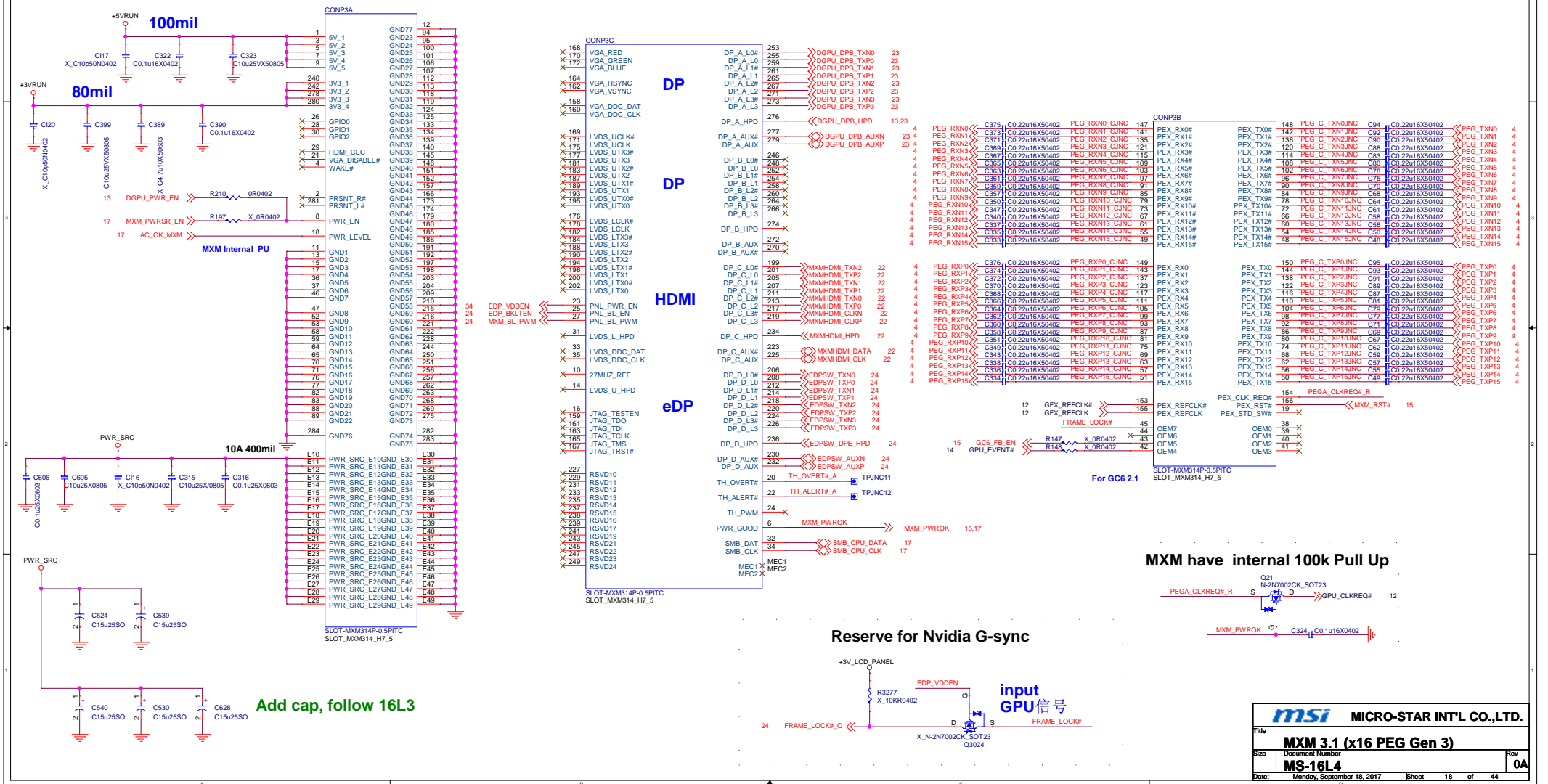
SPI FLASH ROM

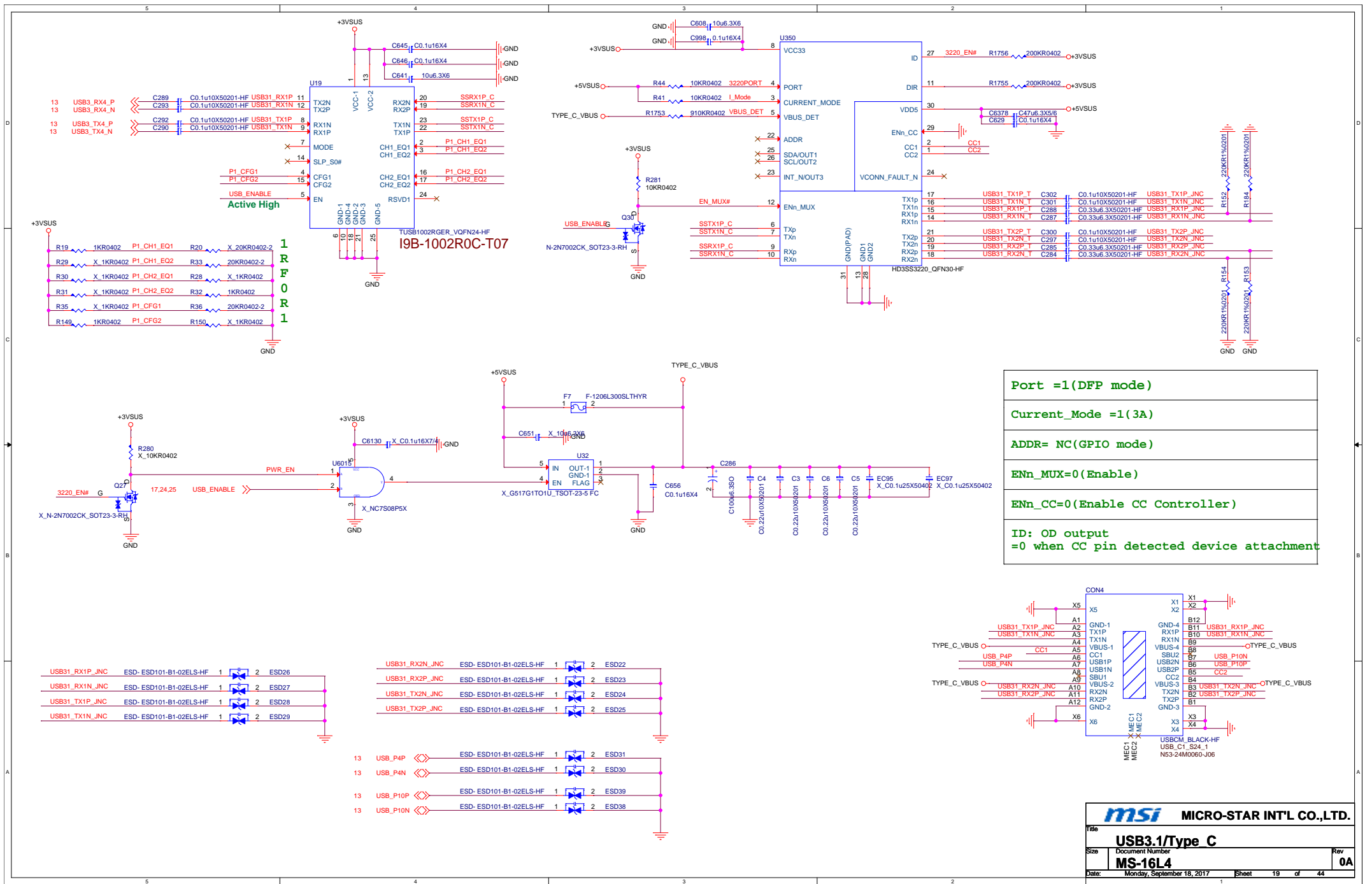


HM370 (Power & GND)

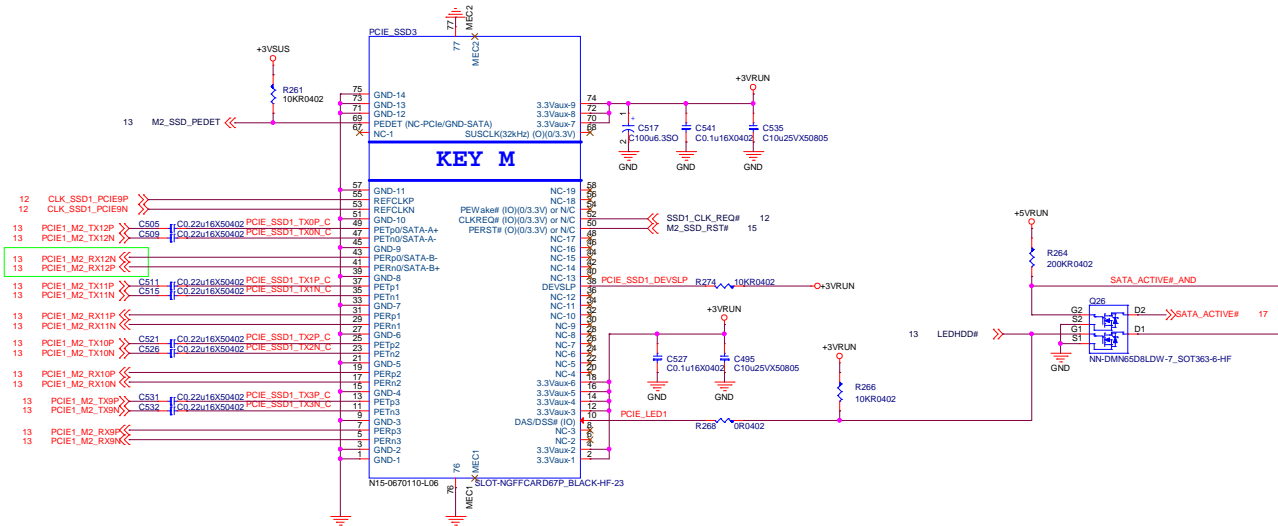


MXM 3.1 (x16 PEG Gen 3)

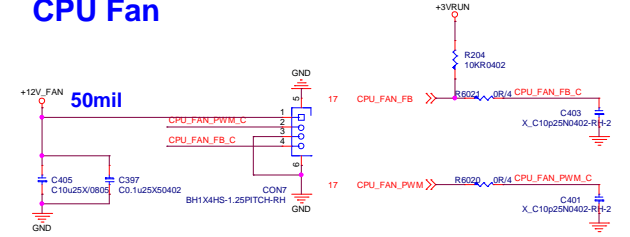




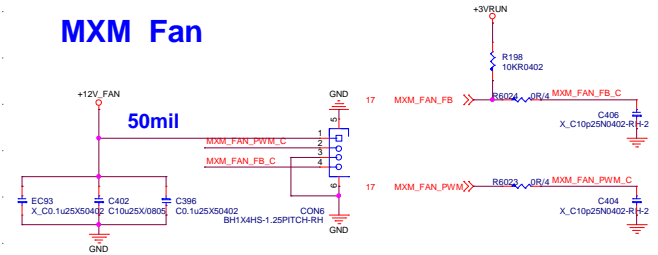
PCIe x4 M.2 SSD



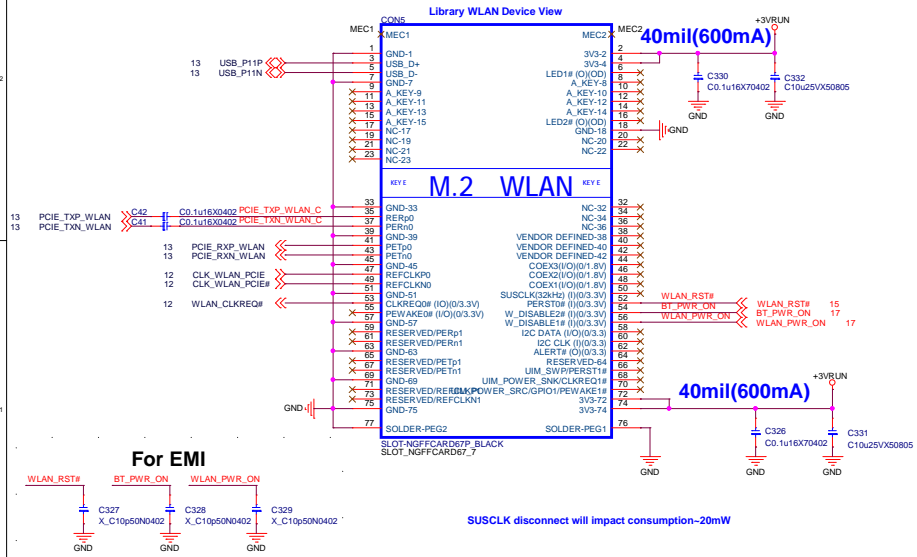
CPU Fan



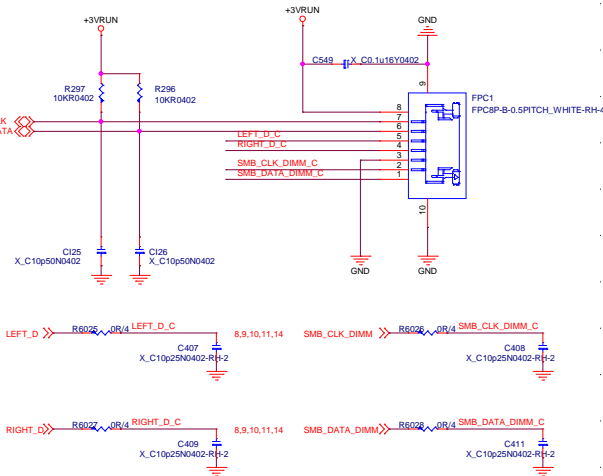
MXM Fan



WLAN/BT

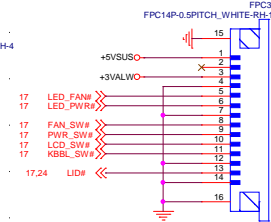


Touch Pad



Launch Board

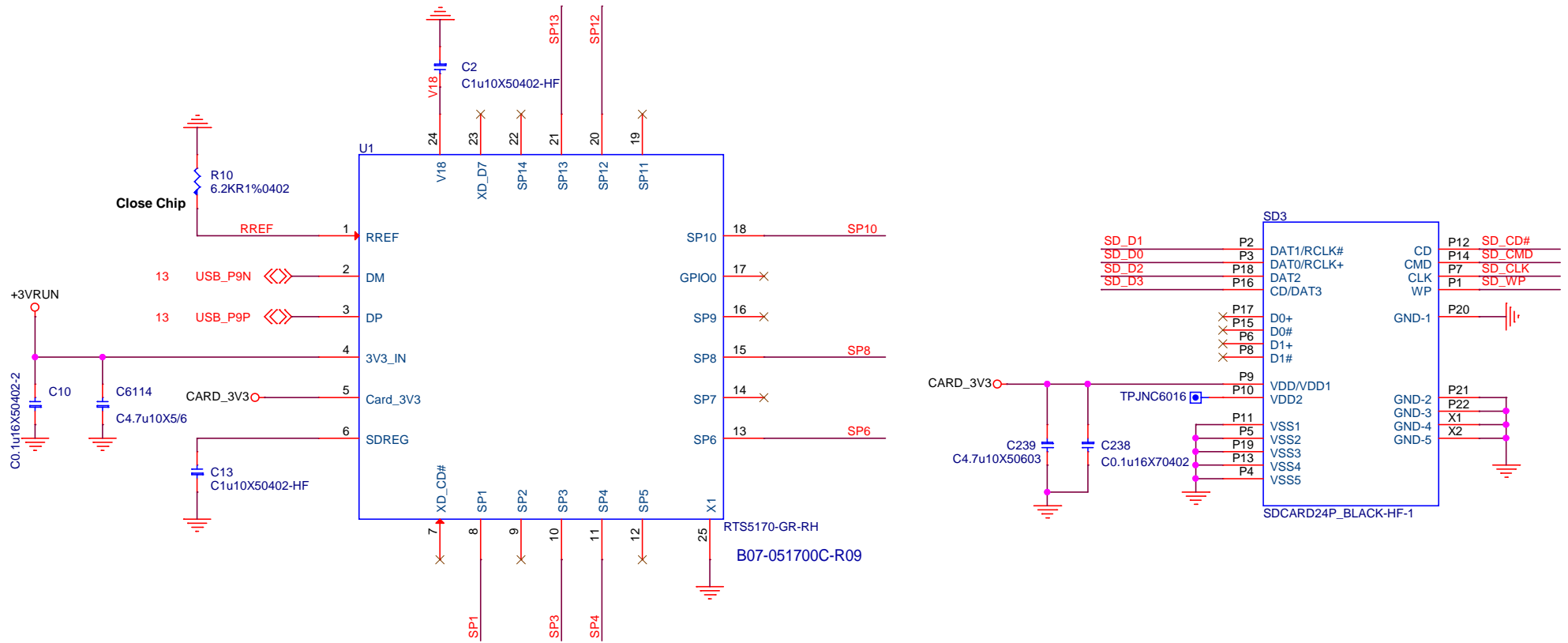
- Power On/Off
- CoolerBoost
- LCD on/off----- Game Caster
- Backlight KB on/off----- SSE



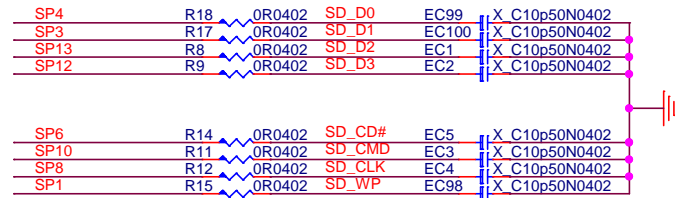
For EMI



Card Reader(RTS5170)



For EMI and Close to RTS5170



SP4	DAT0
SP3	DAT1
SP13	DAT2
SP12	DAT3
SP8	CLK
SP10	CMD
SP6	CD#
SP1	WP

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- 1) remove reserve 181
- 2) change HDMI connector P/N:N5Y-19M0910-AF2

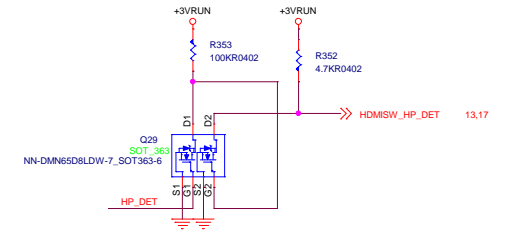
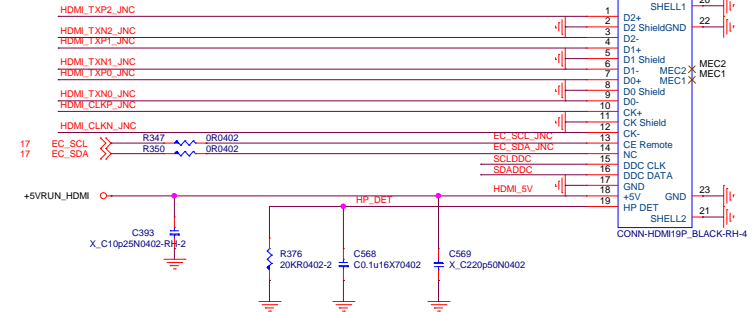

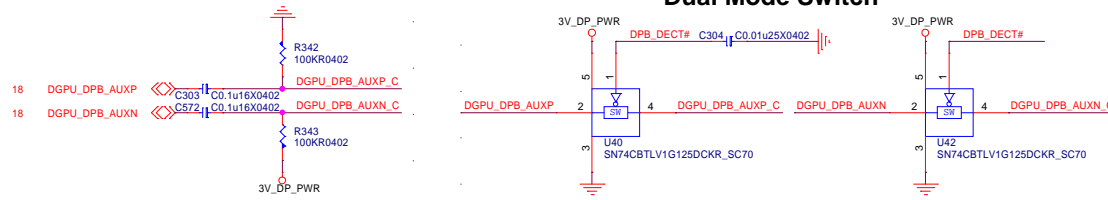


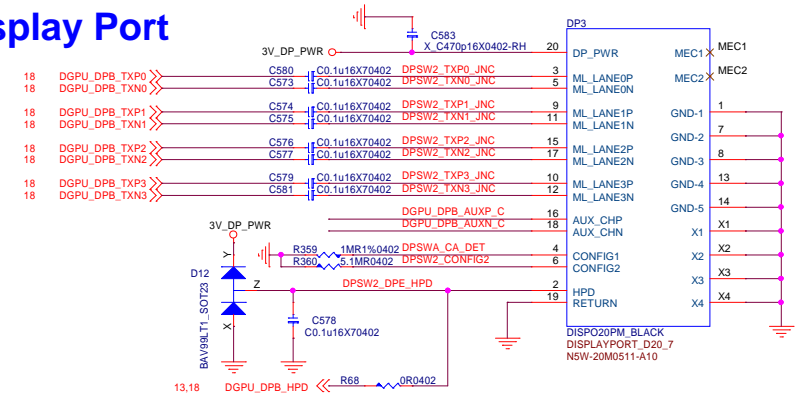
Figure 10 shows four schematic diagrams of HDMI TX pins. Each diagram consists of a horizontal signal line connected to a resistor (R320, R321, R322, or R323) with a value of X_220R1%0402. The pins are labeled HDMI_TXN1_JNC, HDMI_TXN0_JN, HDMI_TXP0_JN, and HDMI_TXP1_JNC respectively.

 MICRO-STAR INT'L CO.,LTD.	
Title	
HDMI 2.0	
Size	Rev
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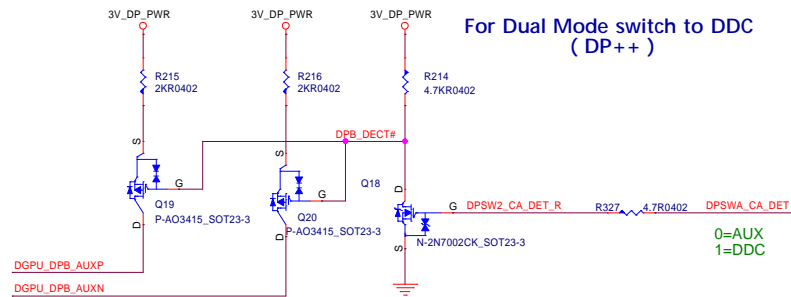
Dual Mode Switch



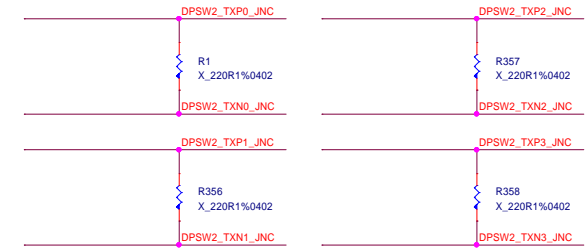
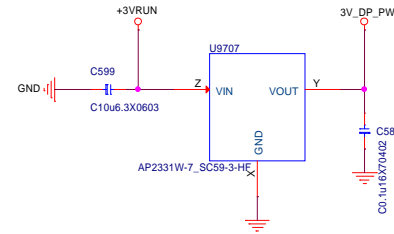
Display Port



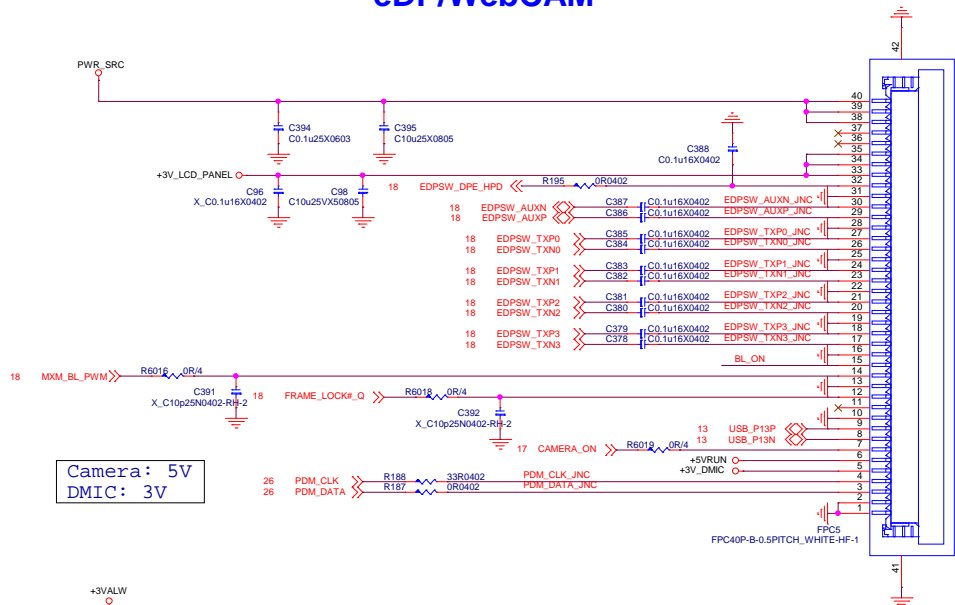
For Dual Mode switch to DDC (DP++)



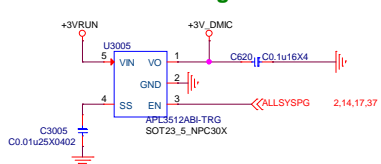
Avoid DP Leakage



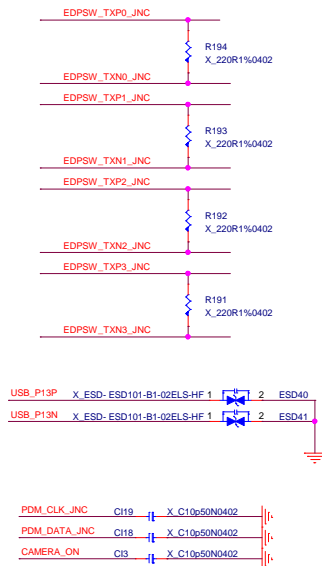
eDP/WebCAM



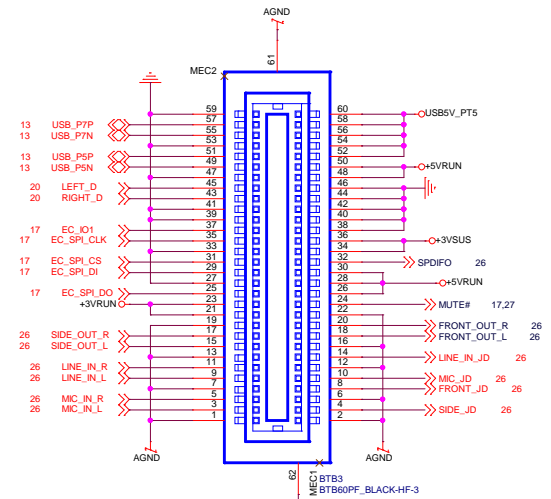
Add DMIC Logic Power



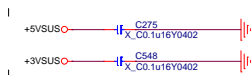
For EMI



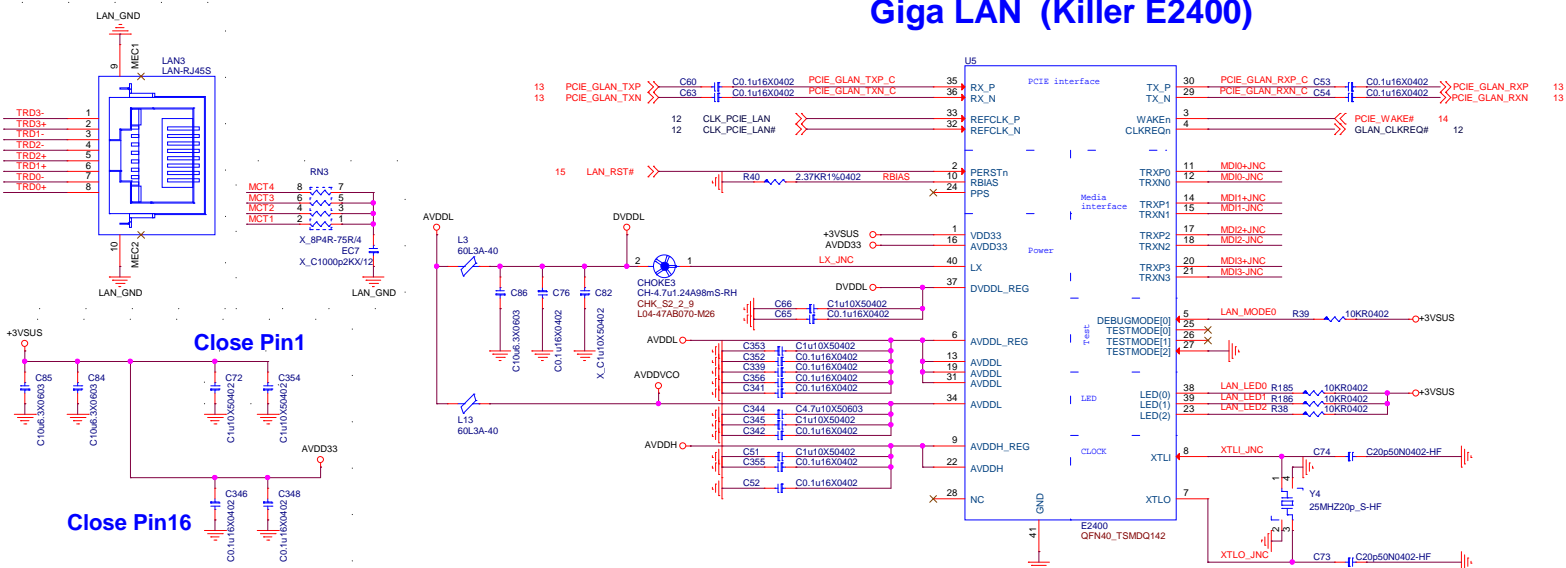
Audio BTB Conn.



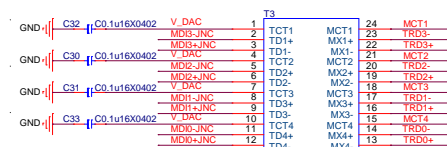
For EMI



Giga LAN (Killer E2400)



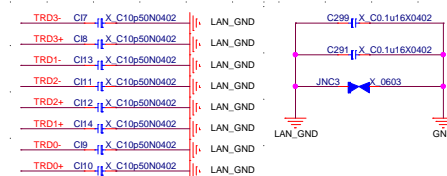
Transfer Mode



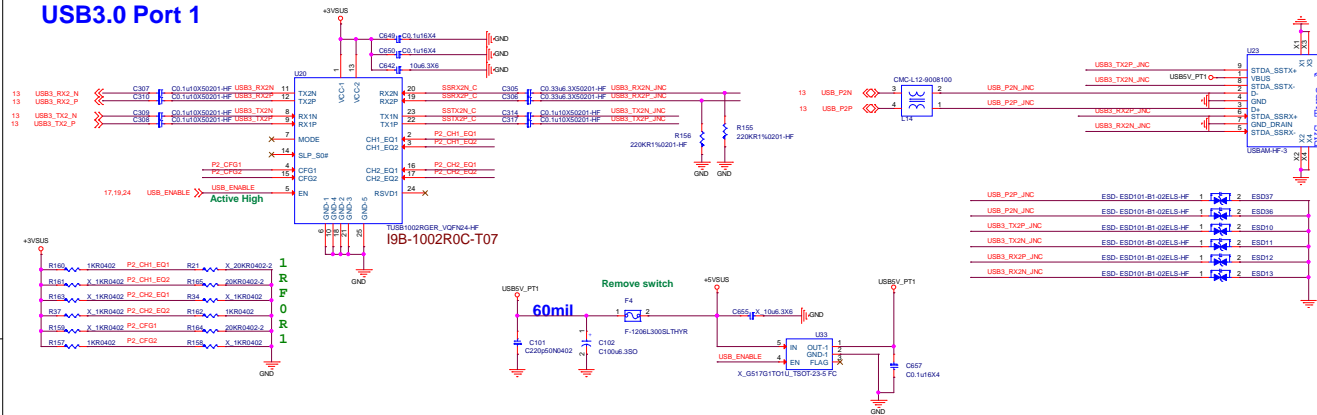
W>20mils



For EMI

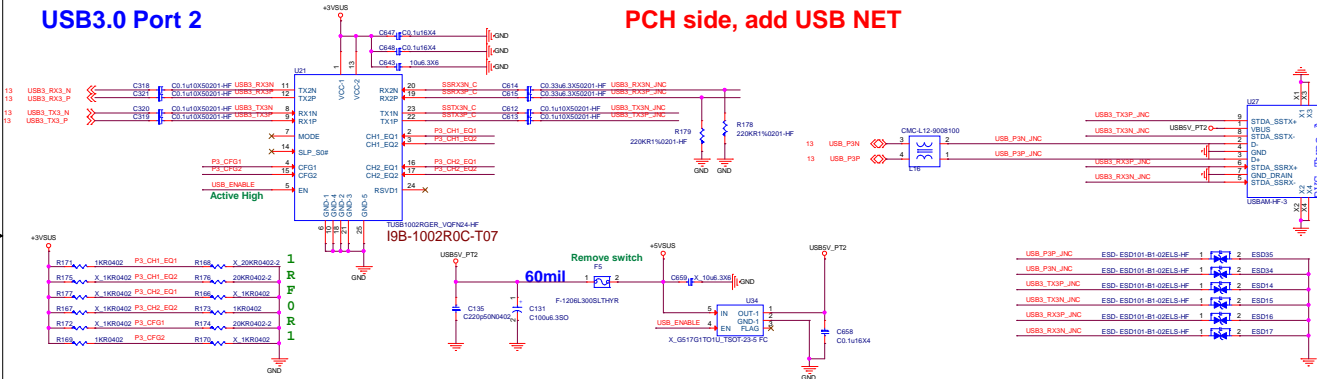


USB3.0 Port 1

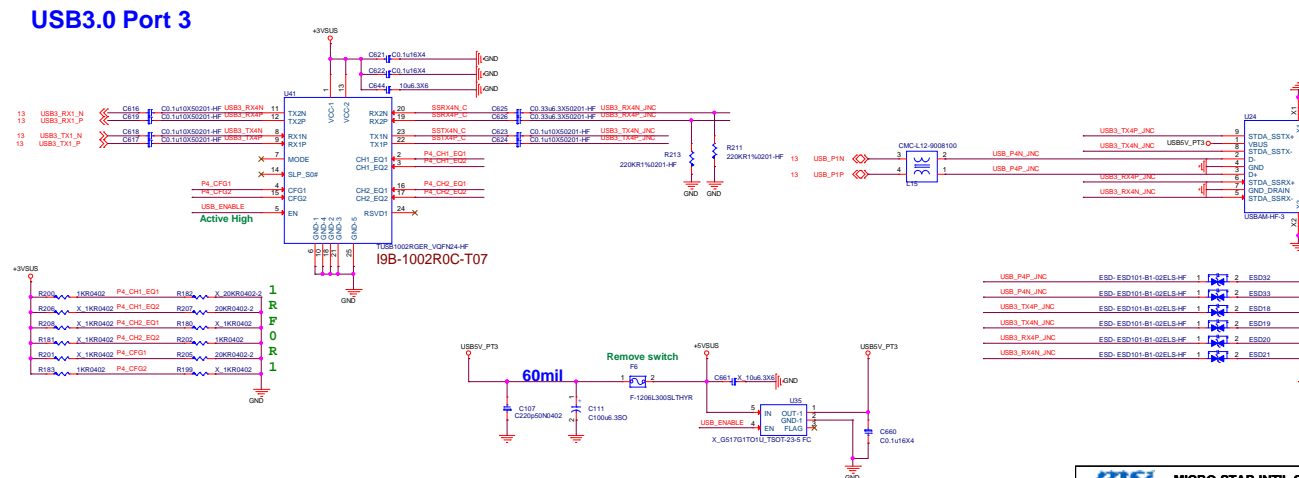


USB3.0 Port 2

PCH side, add USB NET

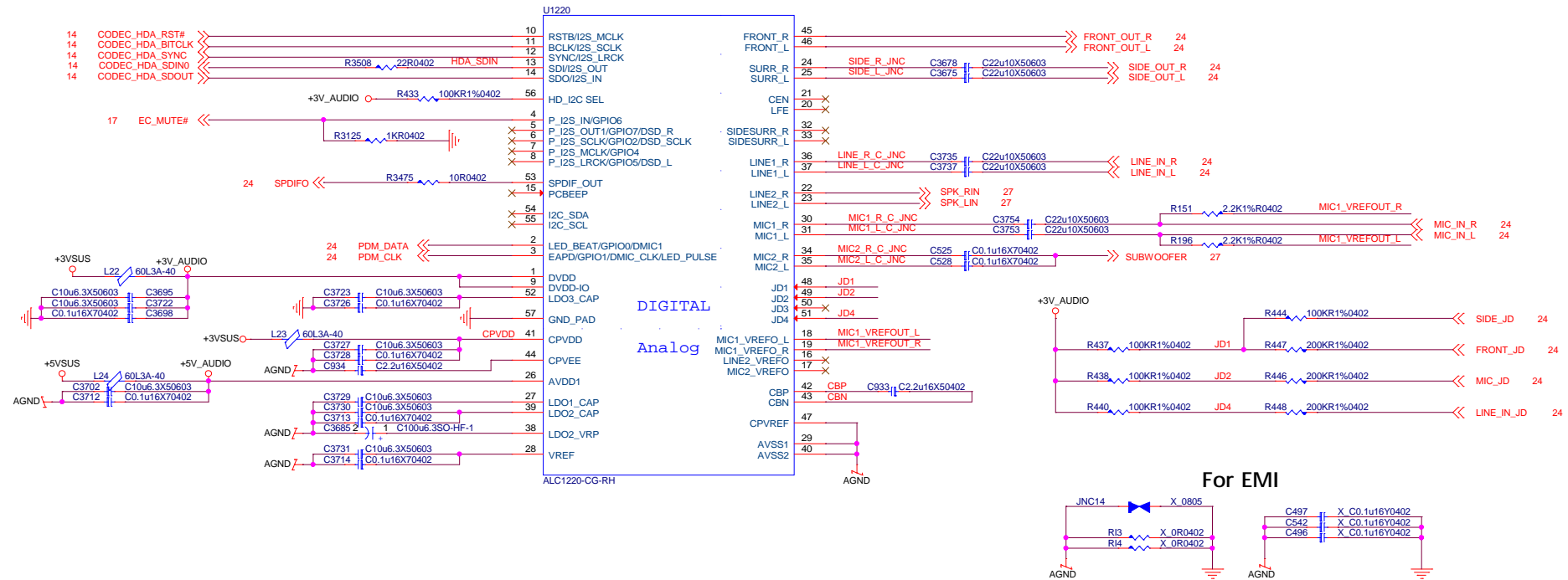


USB3.0 Port 3

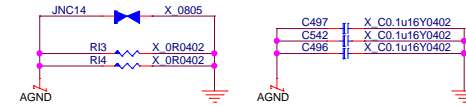


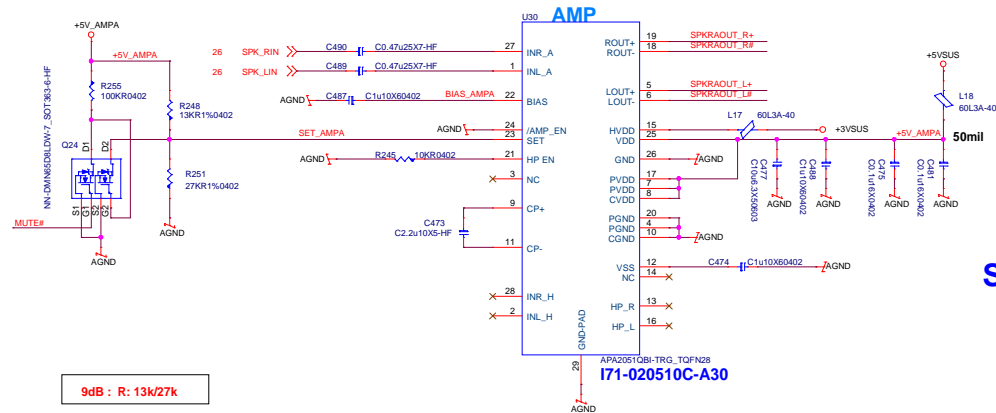
AUDIO(ALC1220)

ALC1220

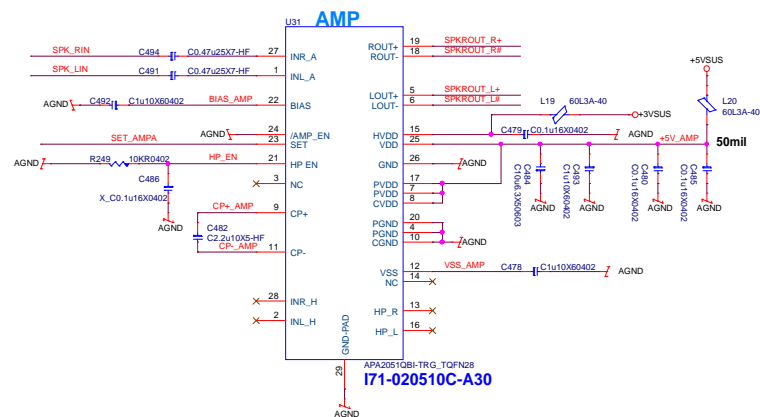
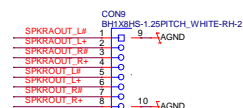


For EMI



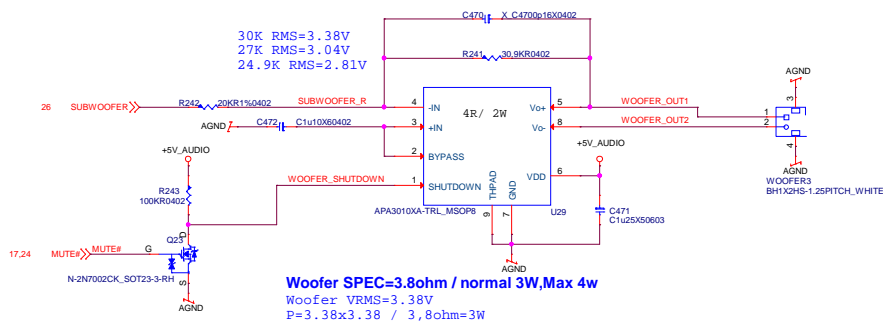


Speaker Output



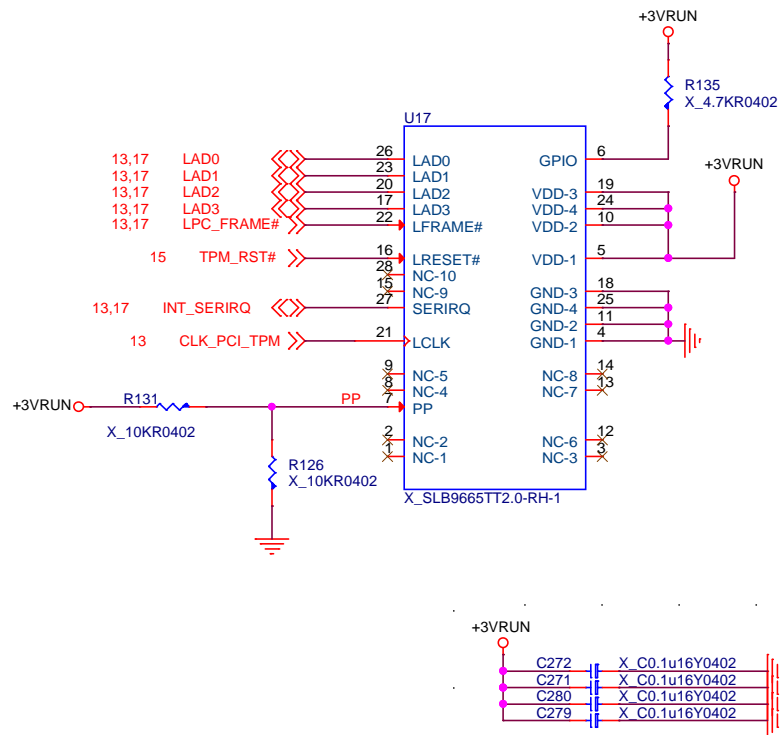
Subwoofer Amp(APA3010)

備註:
C472 改 0402 1uF
C494 C491/C489 C486
改為 0.47 uF

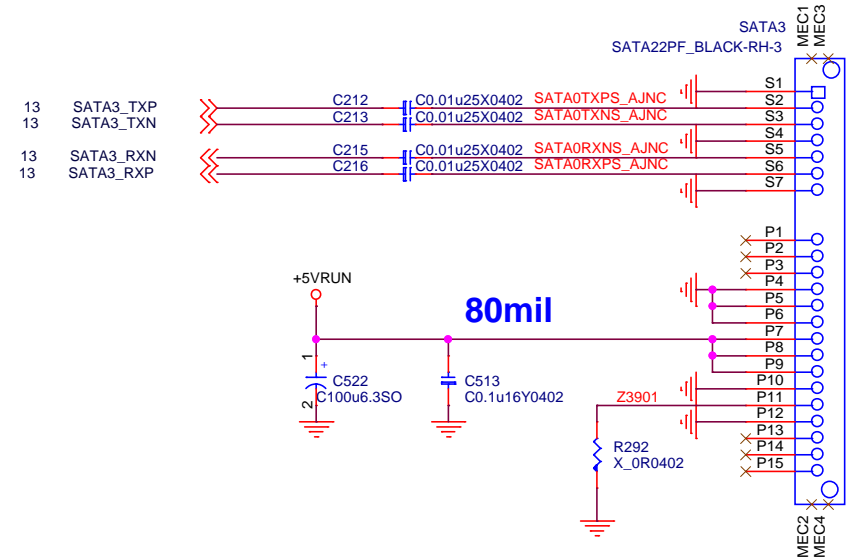


Woofer SPEC=3.8ohm / normal 3W,Max 4w
Woofer: VRMS=3.38V
P=3.38x3.38 / 3.8ohm=3W

TPM



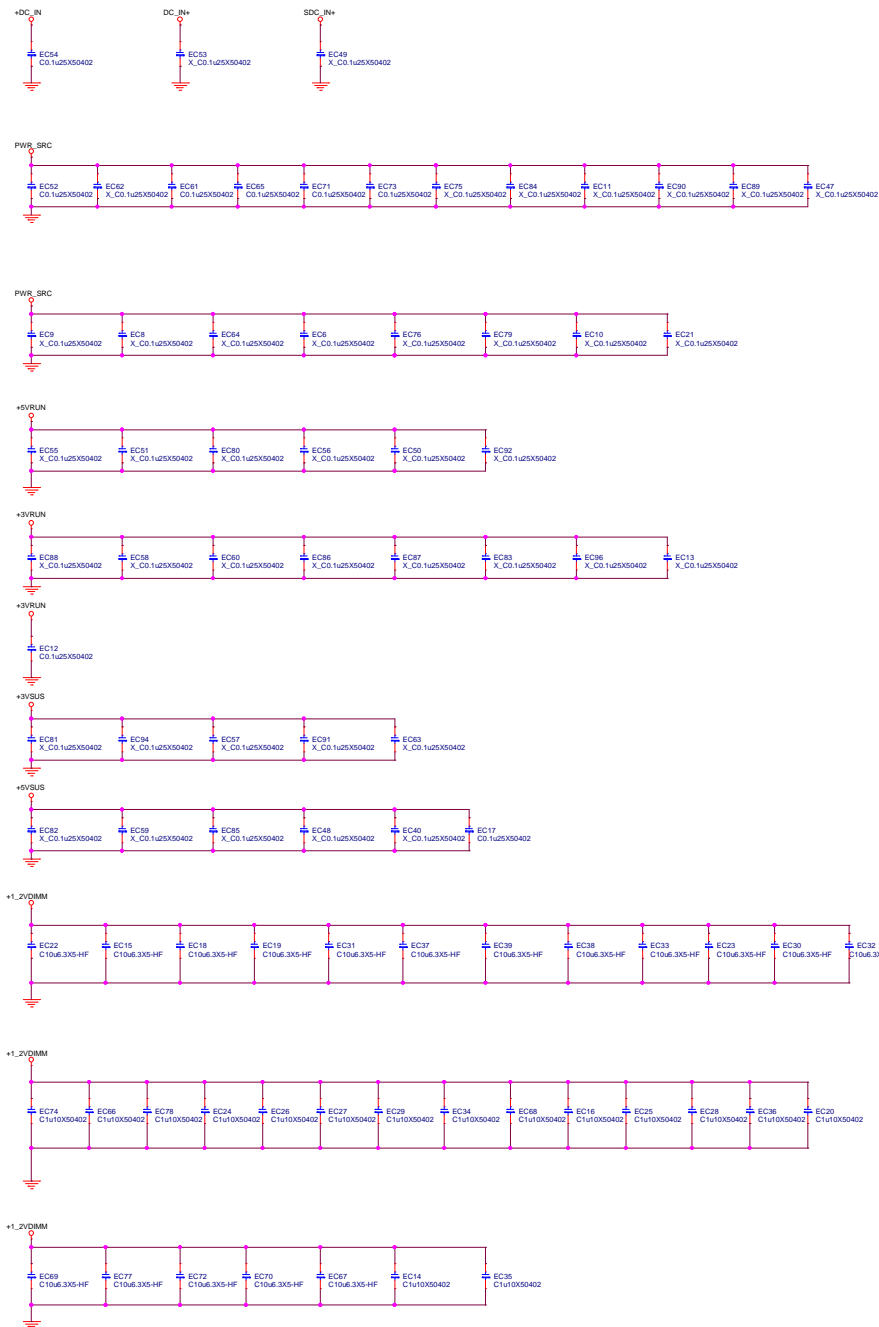
SATA HDD Gen 3



SATA Port change to 4/5

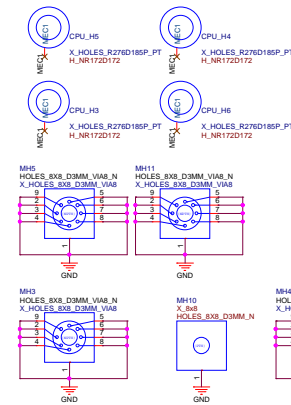
msi MICRO-STAR INT'L CO.,LTD.	
Title	
TPM/HDD	
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EMI



Screw/ME

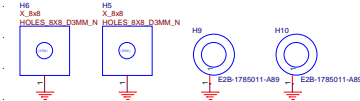
CPU Hole



CPU Bracket



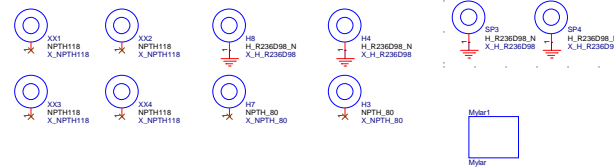
MXM & Fan Stand Off



SSD Stand Off



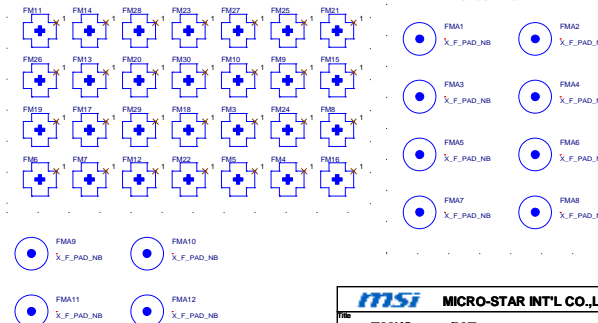
Audio Stand Off



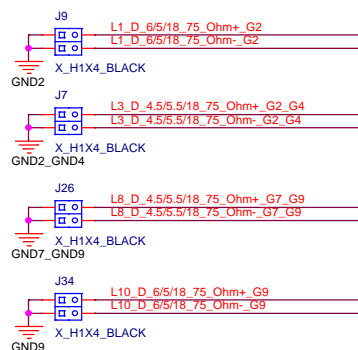
M.2 WiFi Stand Off



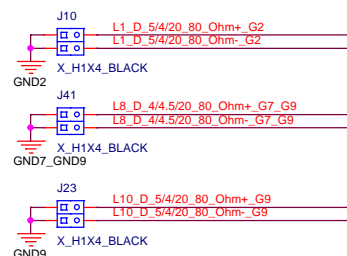
Solder Mark



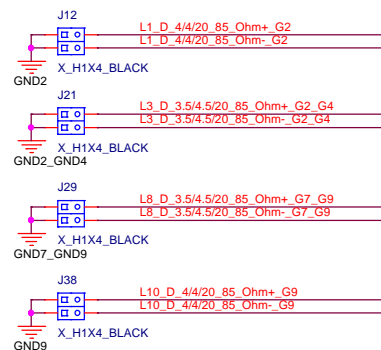
75 OHM / DDR4 DQS



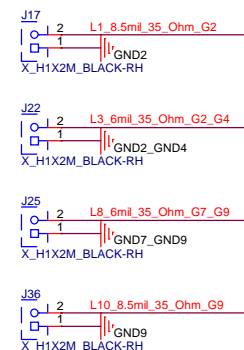
80 OHM / USB3.1



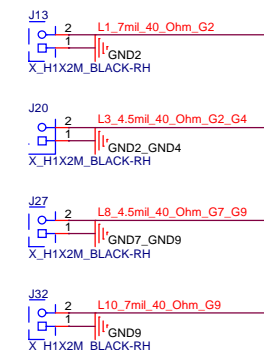
85 OHM /USB,PEG,DMI,CLK



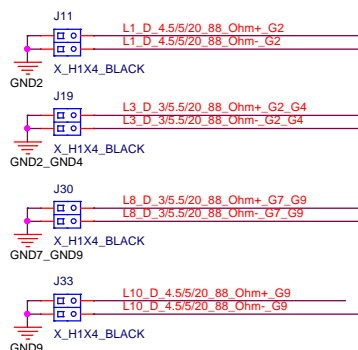
35 OHM / DDR4



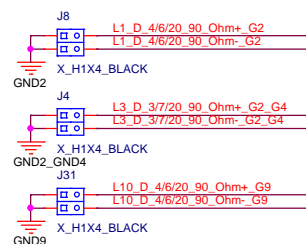
40 OHM / DDR4



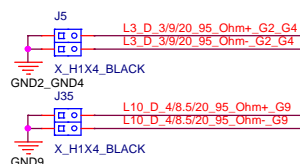
88 OHM / DDR4 CLK



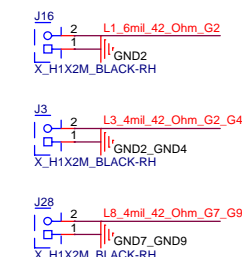
90 OHM / DP,eDP



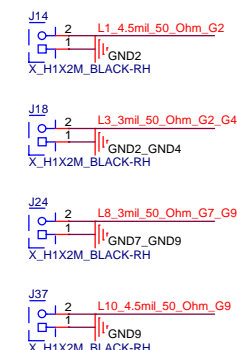
95 OHM / HDMI



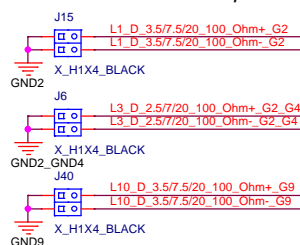
42 OHM / DDR4



50 OHM

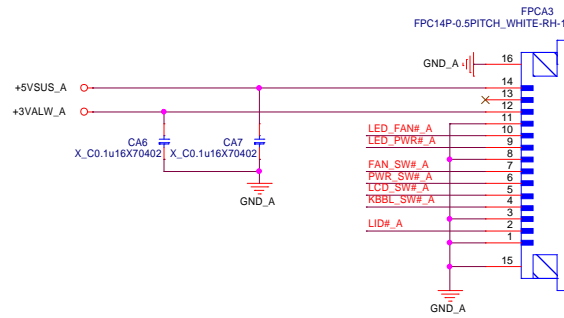


100 OHM / LAN,SD

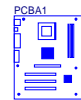
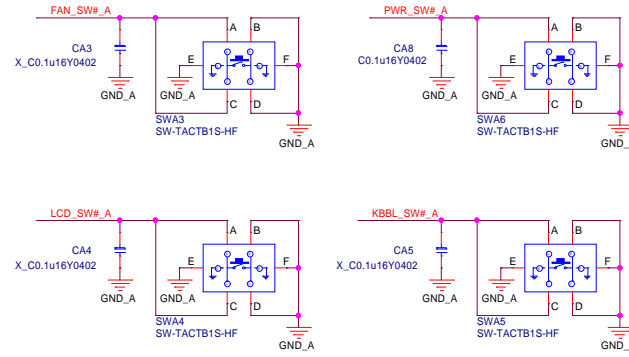


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Title	Standard of impedance
Size	Document Number
	MS-16L4
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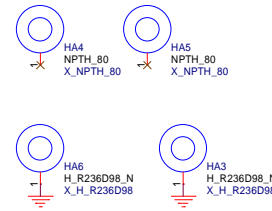
Bottom



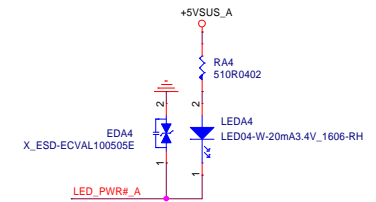
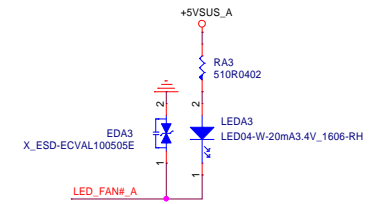
- Power On/Off
- CoolerBoost
- LCD on/off----- Game Caster
- Backlight KB on/off----- SSE



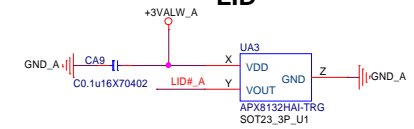
PD0-16L4A0A-H73



LED

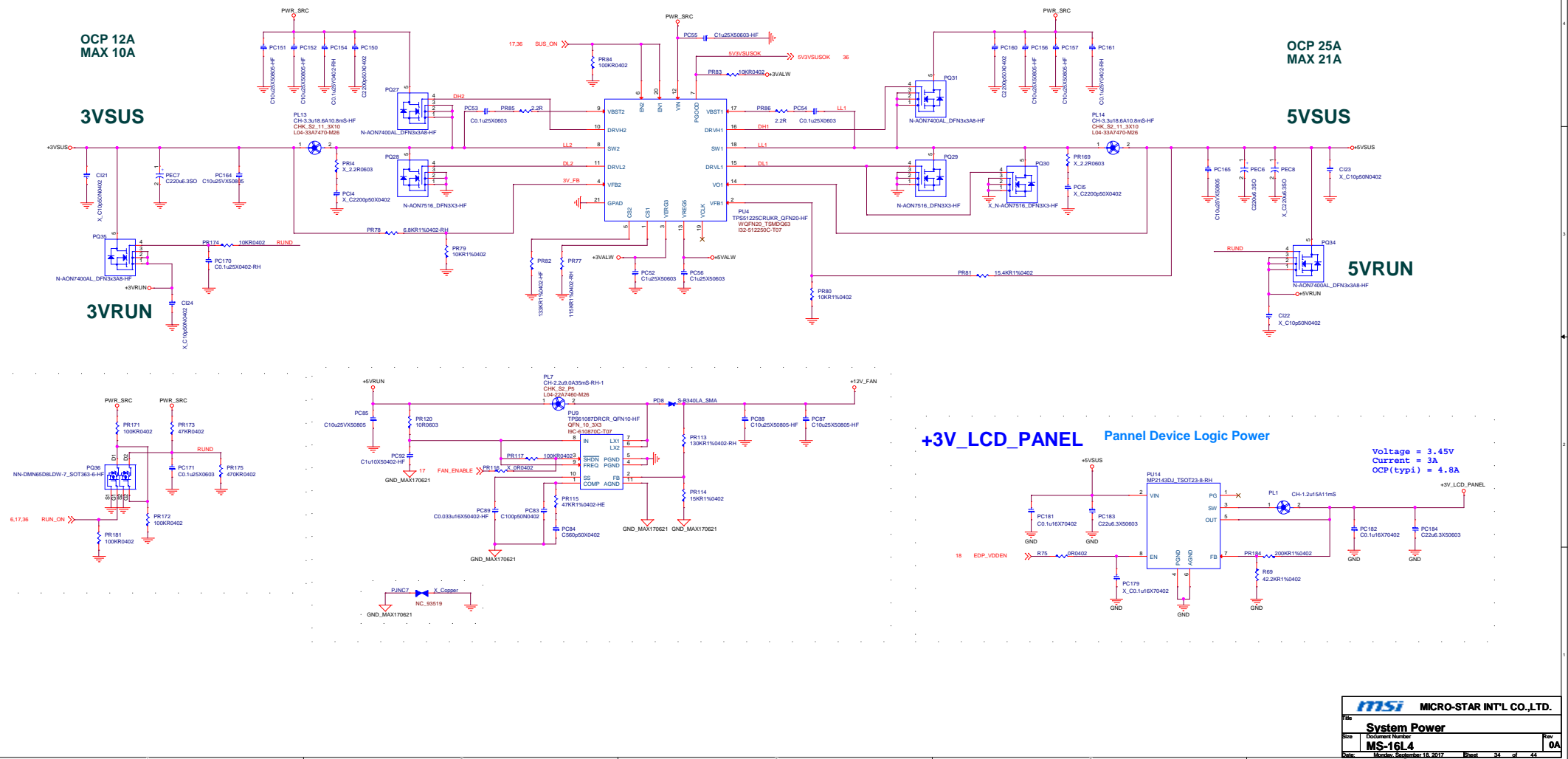


LID

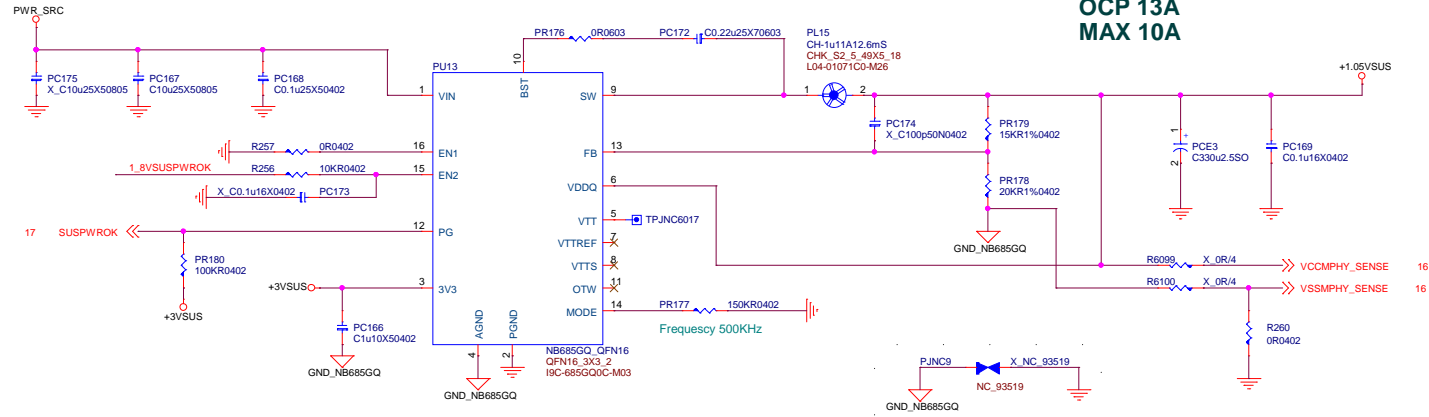


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MS-16L4 Launch Board	
Size	Document Number
MS-16L4	
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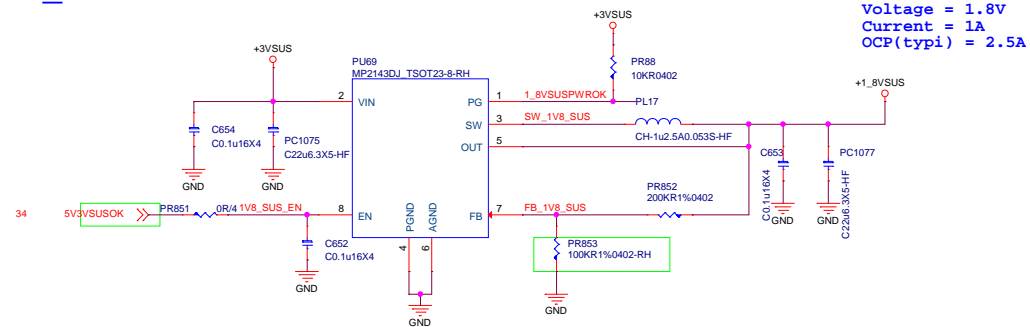
System Power



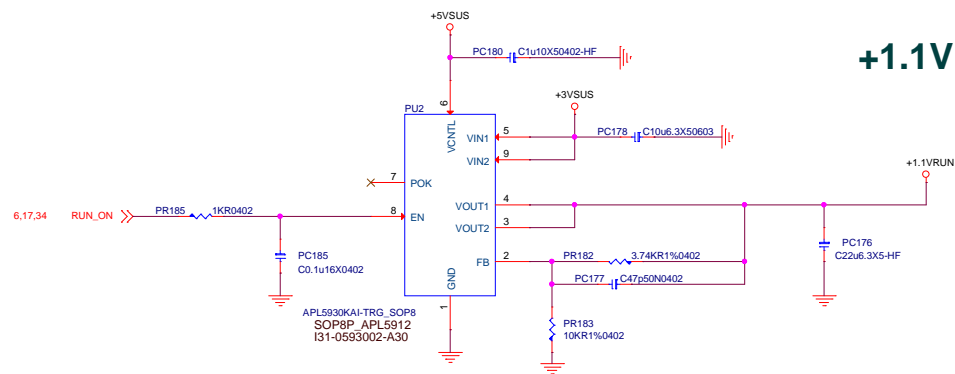
+1.05VSUS OCP 13A MAX 10A



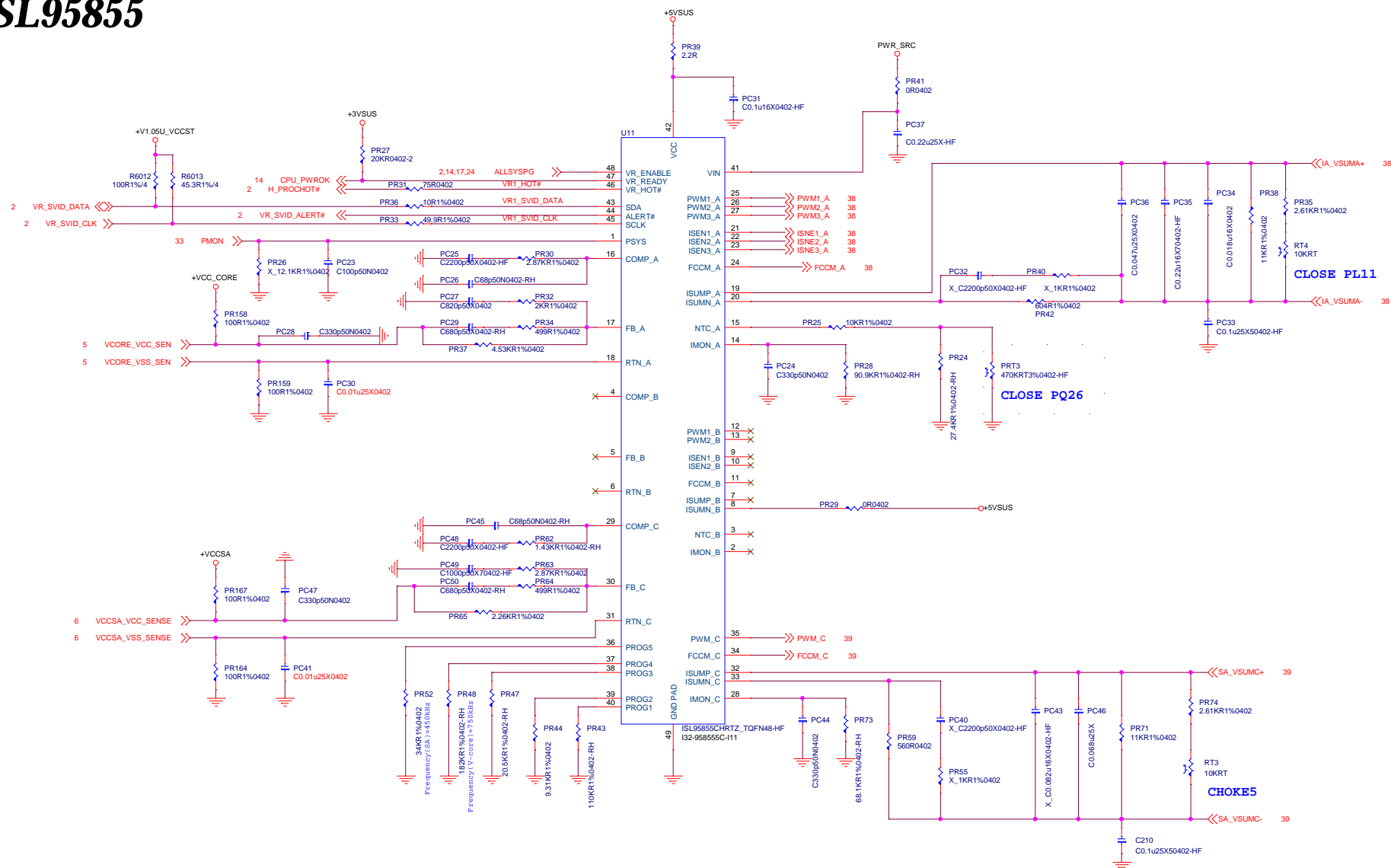
+1_8VSUS



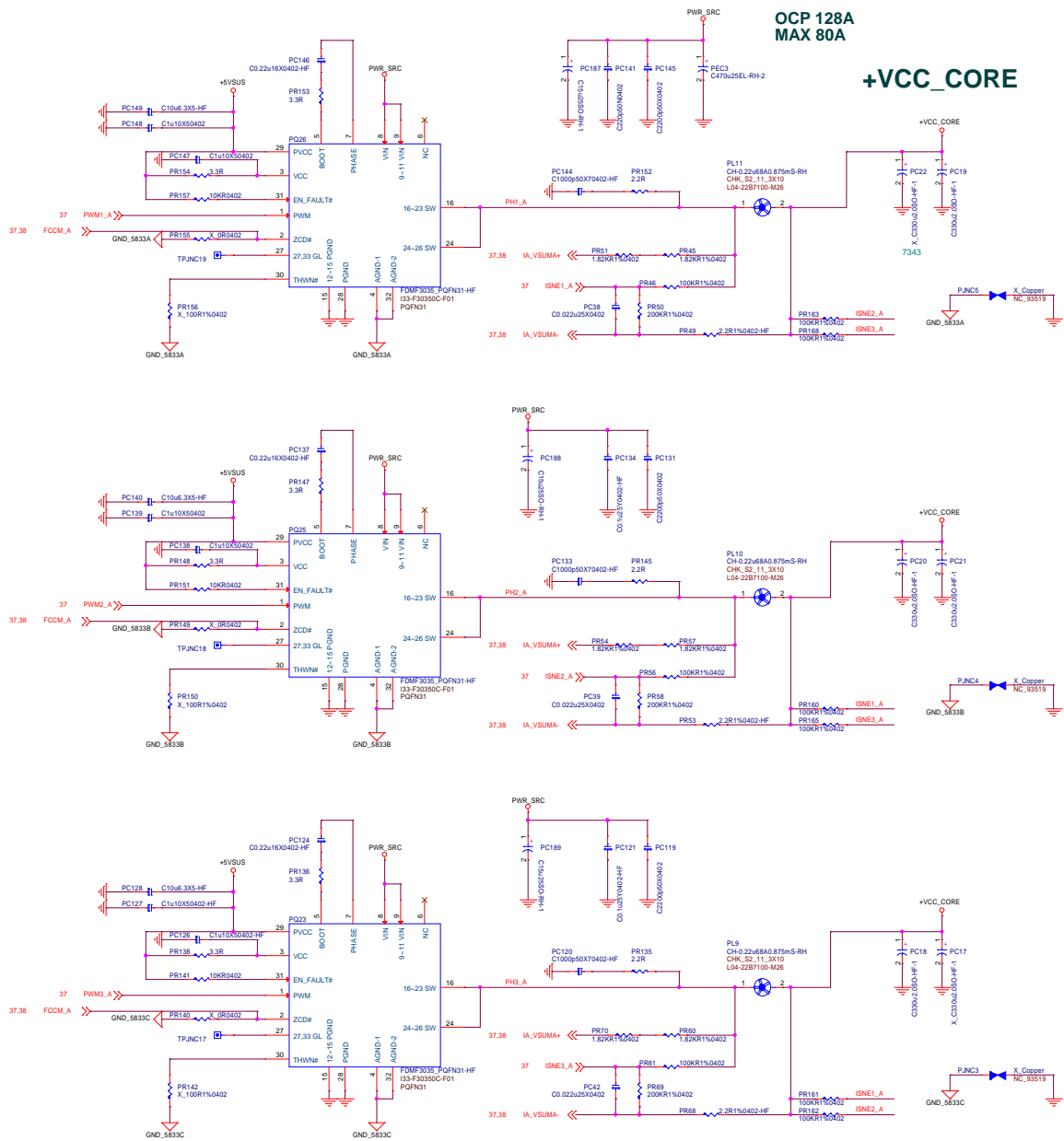
+1.1VRUN



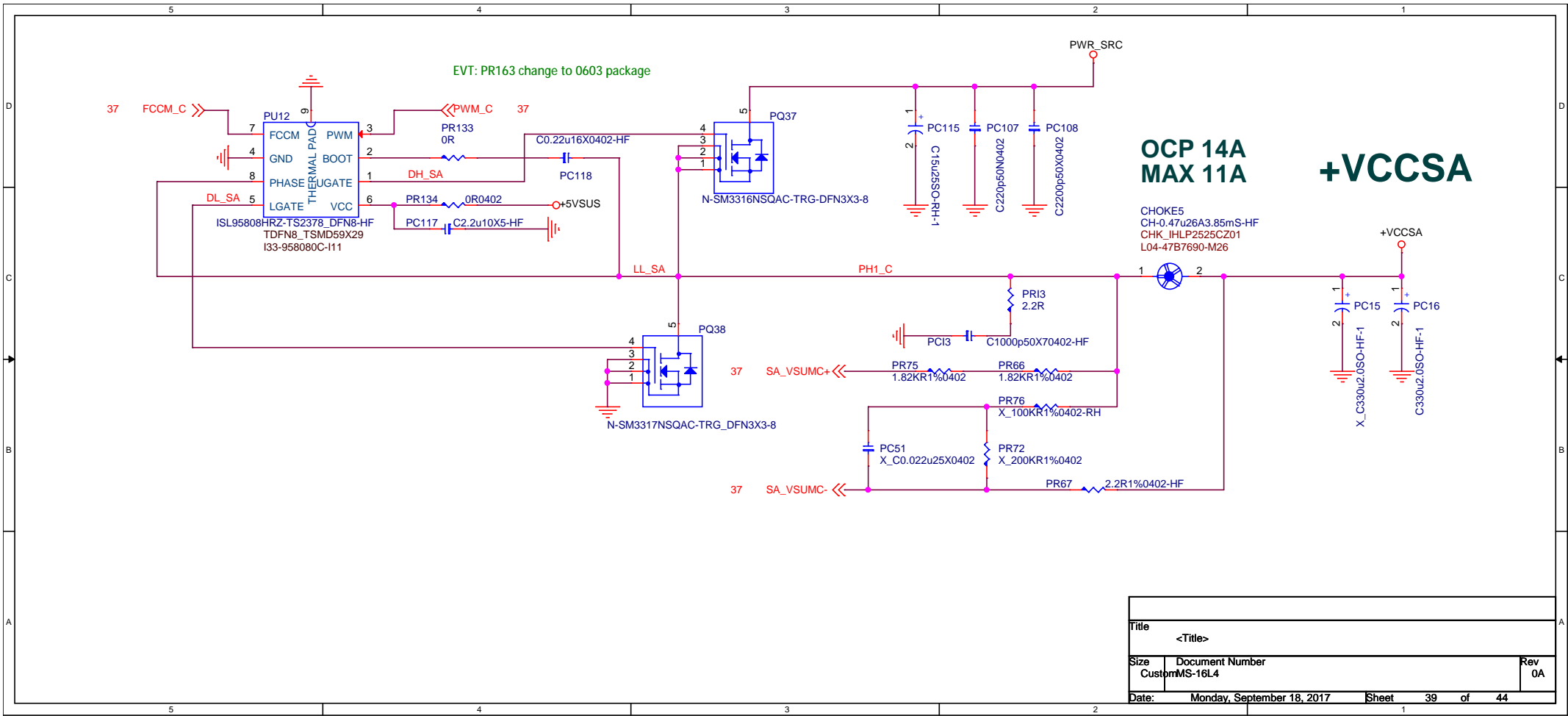
+1.1VRUN stable before 3VRUN:
time: 0--200 μs

Skylake H-line 44e 45W
ISL95855

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+VCCIO
0.95V

6,13 CPU_C10_GATE# R6159 X 0R/4

PWR_SRC +3V RUN PR123 10KR0402

PC96 C10u25X50805-HF PC95 C10u25X50805-HF

VCCIO_EN 5

+3V RUN PR126 10KR0402

+3V RUN PR124 X 10KR0402

PR125 10KR0402

17 VCCIO_PWRGD

3/3

PU10 NB681GD-Z-QFN13-HF QFN13_2X3 I9C-681GD0C-M03

R218 5.1R1%0402-RH-V

PC102 C1u10X50402

GND_NB681A

PR127 0R0402

PR128 3.3R

PC100 C0.22u16X50402-HF

PL8 CH-1u11A12.6mS-HF CHK_S2_5_49X5_18 L04-01071C0-M26

PC129 0R0402

PC103 C0.1u16X0402

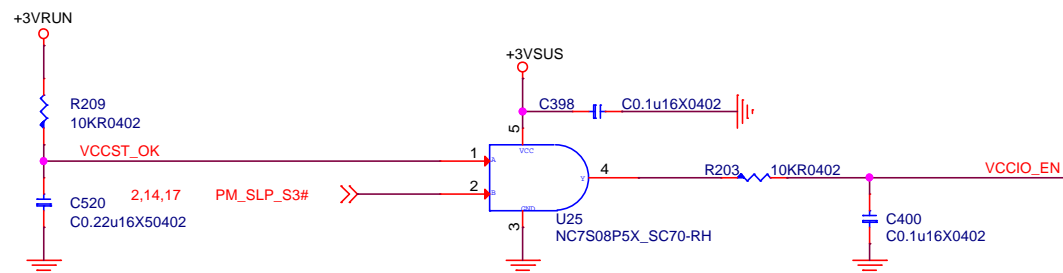
GND_NB681A

C47u6.3X50805-HF

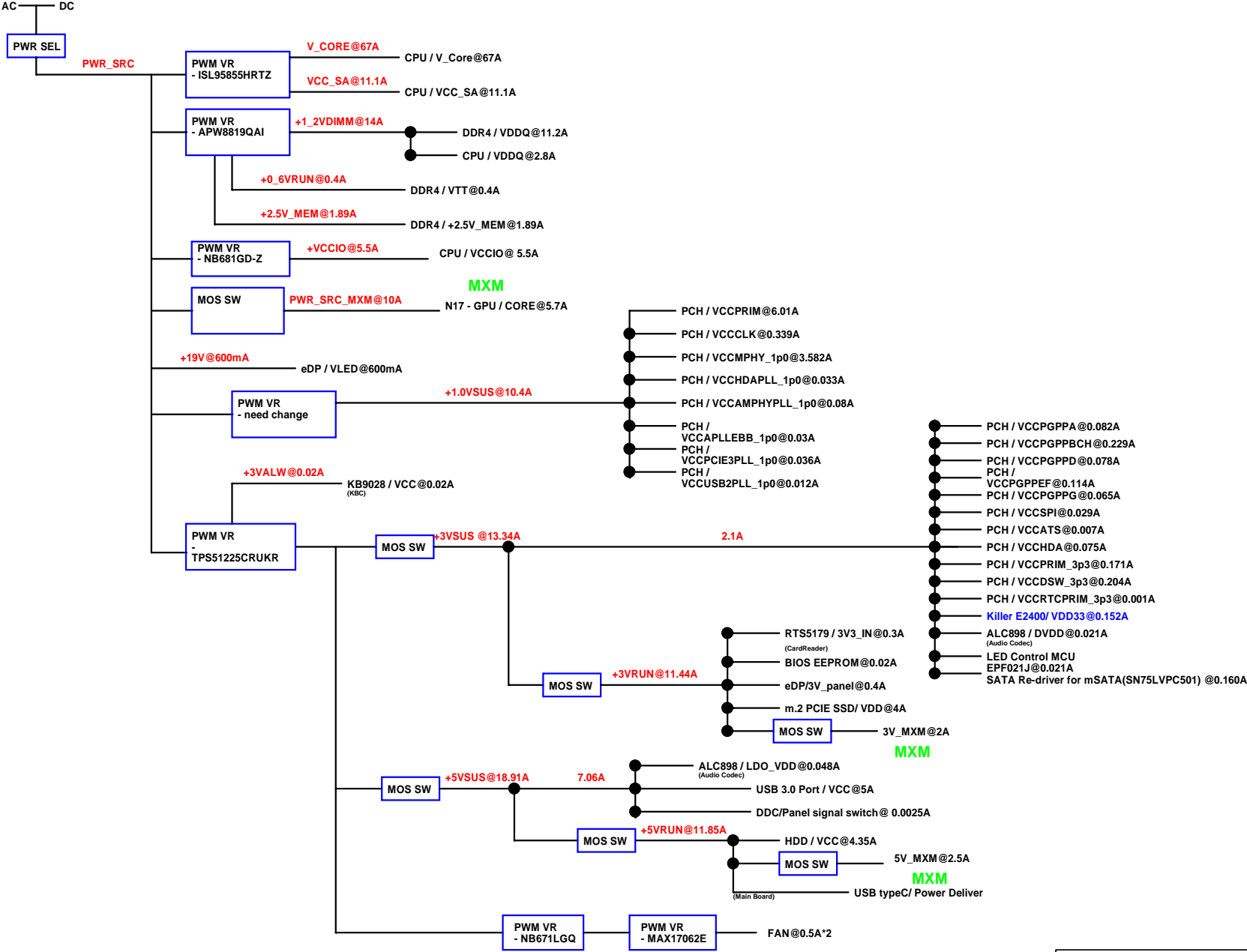
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X_C220u2.55Q-RH-4

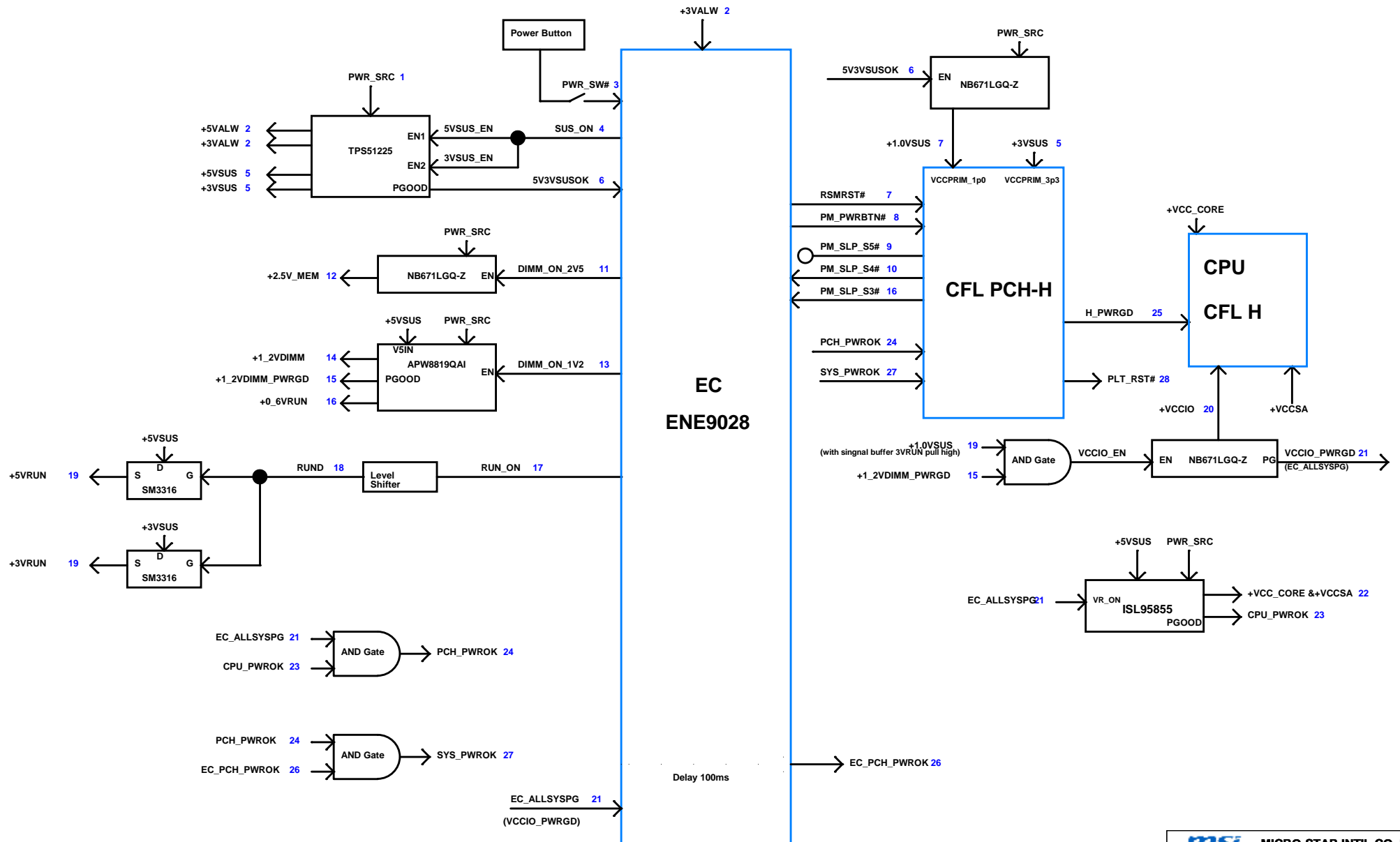
PJC8 X_Copper NC_93519



MS-16L4 Power Delivery Chart

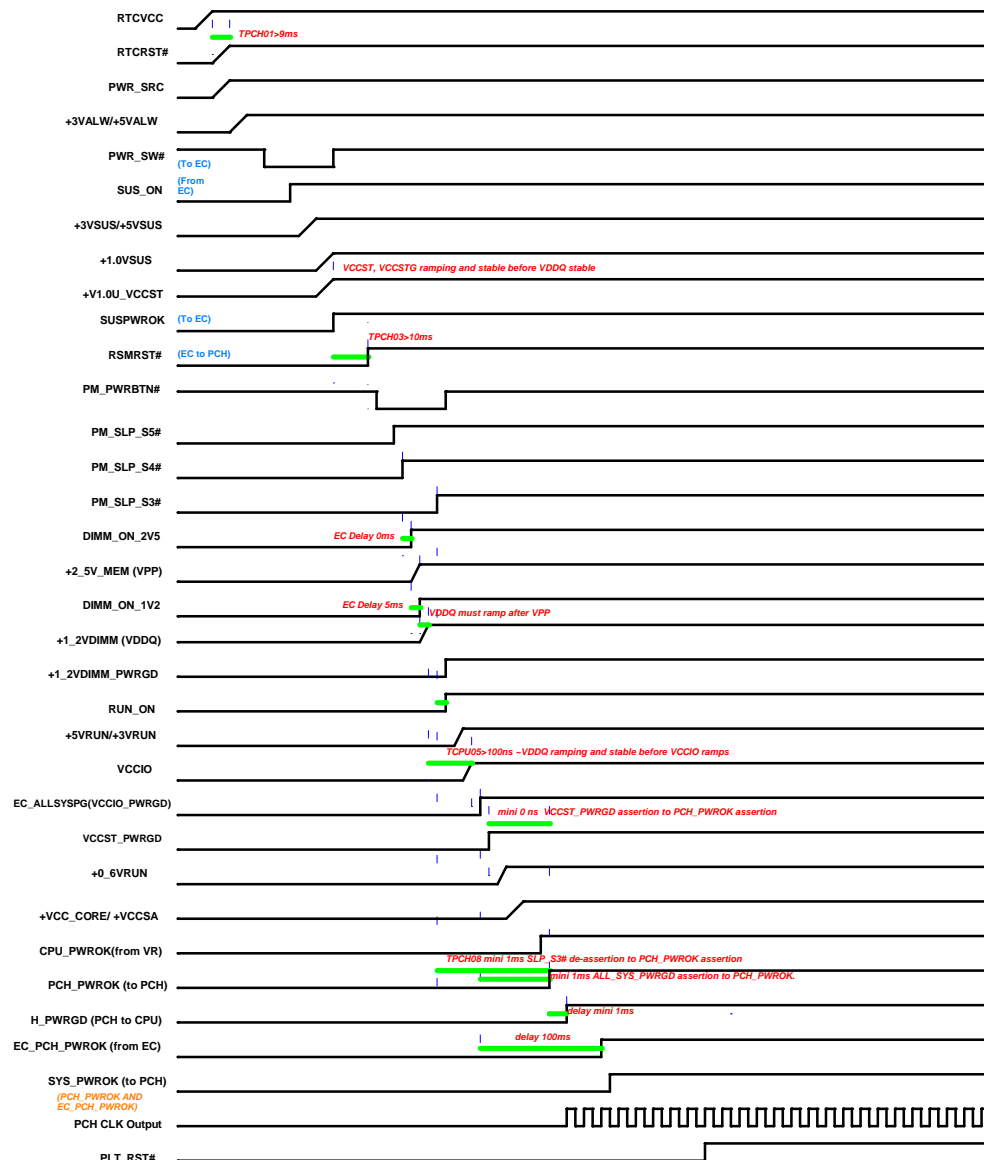


MS-16L4 Power on Block Diagram



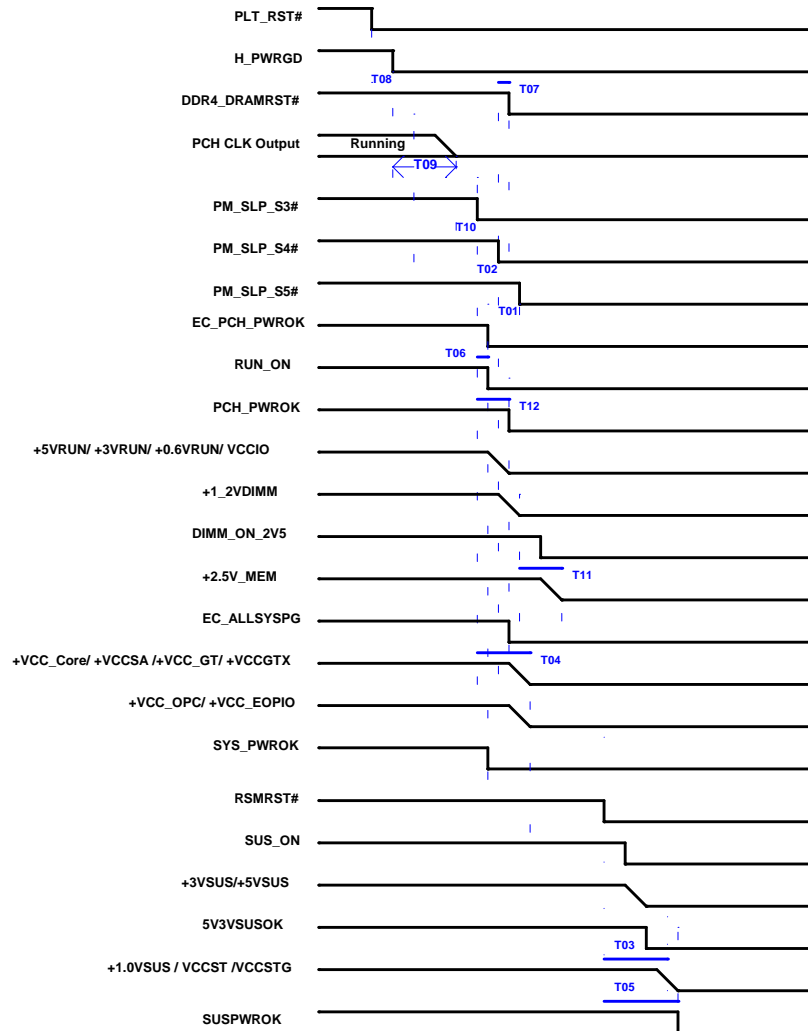
16L2 Power on Sequence

G3 -> S0



Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion